

**(19) World Intellectual Property Organization
International Bureau**



(43) International Publication Date
26 July 2001 (26.07.2001)

(10) International Publication Number
WO 01/53916 A2

PCT

- | | |
|--|--|
| <p>(51) International Patent Classification⁷: G06F 1/10</p> <p>(21) International Application Number: PCT/US01/02642</p> <p>(22) International Filing Date: 24 January 2001 (24.01.2001)</p> <p>(25) Filing Language: English</p> <p>(26) Publication Language: English</p> <p>(30) Priority Data:
 60/177,776 24 January 2000 (24.01.2000) US
 60/182,421 14 February 2000 (14.02.2000) US</p> <p>(71) Applicant (for all designated States except US): BROADCOM CORPORATION [US/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).</p> <p>(72) Inventor; and</p> <p>(75) Inventor/Applicant (for US only): LUTKEMEYER, Christian, A., J. [DE/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).</p> | <p>(74) Agent: BURBACH, Stephen, D.; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).</p> <p>(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.</p> <p>(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Declaration under Rule 4.17:
 — <i>of inventorship (Rule 4.17(iv)) for US only</i></p> <p>Published:
 — <i>without international search report and to be republished upon receipt of that report</i></p> |
|--|--|

Declaration under Rule 4.17:

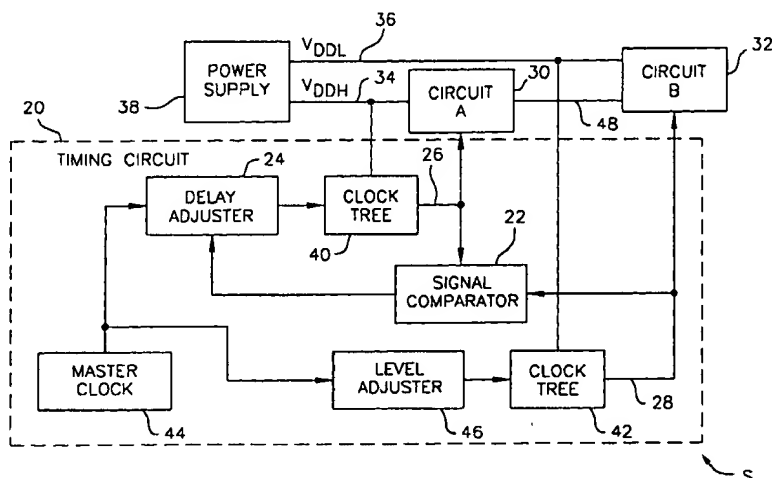
— of inventorship (Rule 4.17(iv)) for US only

Published:

— without international search report and to be republished upon receipt of that report

[Continued on next page]

- (54) Title:** SYSTEM AND METHOD FOR COMPENSATING FOR SUPPLY VOLTAGE INDUCED SIGNAL DELAY MISMATCHES



- (57) Abstract:** Various systems and methods providing signal delay compensation for circuits such as a multi-pair gigabit Ethernet transceiver are disclosed. In an analog implementation a buffer with an adjustable delay may be used to minimize the delay mismatch between clock trees. The delay of the adjustable-delay buffer is controlled by bias voltages that determine the charging and discharging current to the adjustable buffer. A phase detector circuit is used to compare the clock phases for rising and falling edges, and to adjust the bias voltages that control these edges. In a digital implementation a selector switch, responsive to a phase detector, may be used to route clock signals through circuit elements to delay clock signals.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

1 **SYSTEM AND METHOD FOR COMPENSATING FOR SUPPLY**
 VOLTAGE INDUCED SIGNAL DELAY MISMATCHES

FIELD OF THE INVENTION

5 The present invention relates generally to electronic circuits and, more particularly, to efficient clock domain partitioning and clock delay matching.

BACKGROUND OF THE INVENTION

10 There is a perpetual need for increased operating speed in electronics circuits used in electronic equipment. For example, circuit designers are continually developing communication circuits and microprocessors that can send and process data, respectively, at faster and faster rates.

15 However, tradeoffs typically must be made between the speed at which a circuit operates and the power the circuit consumes. In general, a circuit that operates at a higher speed than a comparable circuit will consume more power than that comparable circuit. In many circumstances, there is a practical limit on the amount of power a given circuit can or should consume. For example, increased power consumption typically results in a higher overall cost for the system. Moreover, certain types of electronic circuits such as integrated circuits can only dissipate a limited amount of power. High power consumption may also have other adverse effects on the operation of a circuit such as reducing the reliability of the circuit and adversely affecting the timing relationships in the circuit.

20 It has been observed that in some circuits not all of the circuitry has the same speed requirements. That is, some of the circuitry may operate at slower speeds than other circuitry. In this case, multiple supply voltages may be used to reduce the power dissipation of the integrated circuit. Those circuits that are speed sensitive are driven at a higher supply voltage while the less speed critical circuits are driven at a lower supply voltage. As a result, the less speed critical circuit will consume less power.

25 Typically, signals will be sent between these high-power and low-power circuits. In the case where these signals are referenced to a common system clock signal, the two circuits will be driven by clock signals derived from the common system clock signal. These derived clock signals, in turn, are generated by circuit components that operate at the respective supply voltage. That is, clock signals for the high-power circuits (the high power domain) are generated by circuit components that operate at the high supply voltage. Clock signals for the low-power circuits (the low-power domain) are generated by circuit components that operate at the low supply voltage.

30 As in virtually all electronic circuits, the circuit components that generate the clock signals induce a delay in signals that pass through them. Moreover, the delay of a given circuit component depends, in general, on the supply voltage. In addition, supply voltages may deviate from their nominal values by certain tolerances, for example, +/-10%. As a result of these delays,

1 the clocks that drive the circuit components that operate at different supply voltages may be delayed in time relative to one another. Moreover, this delay in time may vary over time as the supply voltages deviate within their operating tolerances.

5 The misalignment of the clock signals in the different domains due to this delay may result in clock uncertainty. This, in turn, may reduce the available cycle time of the circuit because the clock uncertainty has to be compensated by asynchronous delays when a signal is exchanged between the two domains within one clock cycle. As a result, it may be impossible to double latch the signals. In sum, this misalignment of the clock signals may corrupt data being processed by the circuit.

10 SUMMARY OF THE INVENTION

The invention is directed to systems and methods for providing signals (e.g., clock signals) to circuits driven by different supply voltages. According to the invention, the signals for the circuits driven by the different supply voltages are delayed, as necessary, to reduce the phase difference (i.e., delay) between the signals.

15 One embodiment of a system constructed according to the invention incorporates a buffer with an adjustable delay to reduce the delay mismatch between clock signals driven by clock trees associated with each supply voltage. A phase detector circuit compares the clock phases for rising and falling edges of the clock signals for each supply voltage. The phase detector circuit controls bias voltages that, in turn, control the delay of the adjustable-delay buffer. Thus, one of the signals is delayed until its delay effectively matches the delay of the other signal.

20 Another embodiment of a system constructed according to the invention incorporates a selector circuit that selectively routes the clock signals for the different supply voltages through an appropriate number of circuit elements to adjust the delay of those clock signals. In this embodiment, the selector circuit is controlled by a phase detector that compares the edges of the clock signals for the different supply voltages.

25 Significantly, the circuits in these embodiments may directly compare signals that have different signal levels (e.g., voltage level and voltage swing). Thus, the teachings of the invention may be incorporated to provide very effective circuits for compensating for delay mismatches between different signals.

30 BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims and accompanying drawings, wherein:

35 Figure 1 is a block diagram of one embodiment of a system incorporating delay compensation according to the invention;

Figure 2 is a block diagram of one embodiment of a clock tree;

1 Figure 3 is a schematic diagram of one embodiment of a branch of the clock tree of Figure
2;

 Figure 4 is an exemplary timing diagram for the three clock signals of Figure 2;

 Figure 5 is a block diagram of one embodiment of an analog delay locked loop circuit
5 according to the invention;

 Figure 6 is a schematic diagram of one embodiment of an adjustable delay buffer circuit
according to the invention;

 Figure 7 is an exemplary graph of delay adjustments for the circuit of Figure 6;

 Figures 8A - 8D are exemplary simulation results for the circuit of Figure 6;

10 Figure 9 is a circuit diagram of one embodiment of a rising edge phase detector
constructed according to the invention;

 Figure 10 is a circuit diagram of one embodiment of a falling edge phase detector
constructed according to the invention;

 Figure 11 is a circuit diagram of one embodiment of low pass filters for the circuit of
15 Figure 5;

 Figure 12 is an exemplary timing diagram for the analog delay locked loop circuit of
Figure 5;

 Figures 13A - 13E are exemplary simulation results for the analog delay locked loop
circuit of Figure 5;

20 Figure 14 is a block diagram of one embodiment of a digital delay locked loop constructed
according to the invention;

 Figure 15 is a block diagram of an alternative embodiment of a circuit for implementing
a variable delay in a digital delay locked loop;

 Figure 16 is a simplified block diagram of one embodiment of a high-speed bidirectional
25 communication system;

 Figure 17 is a simplified block diagram of one embodiment of a giga-bit transceiver
integrated circuit incorporating clock delay compensation according to the invention; and

 Figure 18 is a simplified block diagram of one embodiment of a trellis decoder circuit
incorporated in the integrated circuit of Figure 17.

30

DETAILED DESCRIPTION OF THE INVENTION

 The invention is described below, with reference to detailed illustrative embodiments. It
will be apparent that the invention can be embodied in a wide variety of forms, some of which
may be quite different from those of the disclosed embodiments. Consequently, the specific
35 structural and functional details disclosed herein are merely representative and do not limit the
scope of the invention.

 Figure 1 is a block diagram of one embodiment of a system S utilizing clock delay
compensation in accordance with the present invention. Specifically, the system S incorporates

1 a timing circuit 20 that includes a signal comparator 22 (e.g., a phase comparator) and a delay
adjuster circuit 24 for reducing phase mismatches between clocks 26 and 28 that drive circuit A
30 and circuit B 32, respectively.

5 The system of Figure 1 typically is implemented in an integrated circuit where multiple
supply voltages are used to reduce the power dissipation of the integrated circuit. In this case,
less timing-critical parts operate on a lower supply voltage than timing-critical parts of the circuit.
For example, in Figure 1 each of the circuits 30 and 32 is powered by a different supply voltage
(V_{DDH} 34 and V_{DDL} 36). In practice, a single power supply or more than one power supply 38
may be used to generate supply voltages 34 and 36.

10 As mentioned above, the circuits 30 and 32 may be driven by different clock signals 26
and 28. Typically, clock trees are used to buffer a master clock signal to provide clock signals
with sufficient current drive to the circuits. In Figure 1, the master clock signal drives two clock
trees, one buffer tree in the high voltage domain, and the other buffer tree in the low voltage
domain.

15 A clock tree 40 generates the clock signals 26. As shown in Figure 1, the clock tree 40
is powered by supply voltage V_{DDH} 34 so that the clock signals 26 have the appropriate signal
level (e.g., voltage level and swing) for circuit A 30. In this embodiment, the clock signal is
generated by a master clock 44 that is powered by supply voltage V_{DDH} 34.

20 A clock tree 42 generates the clock signals 28. The clock tree 42 is powered by supply
voltage V_{DDL} 36 so that the clock signals 28 have the appropriate signal level (e.g., voltage level
and swing) for circuit B 32. To this end, a level adjuster 46 is provided to shift the level of the
clock signal generated by the master clock 44 to a level compatible with circuits powered by
supply voltage V_{DDL} 36.

25 Figure 2 illustrates one implementation of the clock trees 40 and 42. As represented in
Figure 2, both clock trees are driven by a common clock signal designated ϕ . Clock tree 40
generates a set of clock signals designated ϕ_{iH} . Clock tree 42 generates a set of clock signals
designated ϕ_{iL} . Clock tree 40 has a supply voltage V_{DDH} of 2.5 volts. Clock tree 42 has a supply
voltage V_{DDL} of 1.8 volts. Either of these supply voltages may vary by +/-10% due to temperature
and other variants.

30 Figure 3 illustrates how the clock signal ϕ may be delayed as it passes through each of
the components in a clock tree. The schematic at the top of Figure 3 represents one embodiment
of a branch of the clock tree 42 along with the level adjuster 46. Each branch of the clock tree
includes several buffers, the number of which will depend, in part, on the number of branches
required for the clock tree and the current drive capability of the buffers. The level adjuster 46
35 converts the signal level of the clock signal from the 2.5 volt range to the 1.8 volt range.

The chart immediately below the schematic in Figure 3 illustrates delay characteristics of
the clock tree 42 and the level adjuster 46. The symbols SS, TT and FF represent simulations at
the slow slow, typical typical and fast fast corners, respectively (e.g., worst case, typical case and

1 best case scenarios). Each row in the chart sets forth the delays (in nanoseconds, nS) for a given
part of the branch. For example, for the typical case, the dispersed buffer cell 50 has a delay of
0.26 nS. The level adjuster 46, nor gate 52, inverter 54 and buffer 56 have a total delay of 1.02
nS. The nor gate 58, inverter 60 and buffer 62 have a total delay of 0.72 nS. Thus, the total delay
5 for the branch is 2.00 nS.

The delay of these buffers is supply voltage dependent. In other words, when the supply
voltage in a given domain changes, the delays of the buffers may change. This scenario is
illustrated in Figure 4 which depicts exemplary timing diagrams for the three clock signals, ϕ ,
 ϕ_{Ht} and ϕ_{Lt} . Under typical conditions, the circuit may be designed so that ϕ_{Ht} and ϕ_{Lt} are
10 delayed by approximately the same amount of time, τ_{Ht} and τ_{Lt} respectively. However, when
one of the supply voltages changes (e.g., V_{DDH} decreases by 10%), the delay through the
corresponding buffer tree (e.g., buffer tree 40) may increase (e.g., by 12%). This situation is
indicated graphically in Figure 4 as edges of the clock signal moving in time either to the left or
right.

15 Significantly, the supply voltages may change independently of each other. Thus, even
if the clock trees are nominally designed to have the same delay, under normal operating
conditions the actual delay of the clock trees may be mismatched by several hundred
picoseconds. This may occur, for example, when one supply voltage is at its maximum value and
the other is at its minimum value. Under these worst case conditions the edges of the clock
20 signal might move in time either to the left or right by the maximum amounts indicated in Figure
4 (e.g., $\tau_{Ht} +12\%/-8\%$; $\tau_{Lt} +21\%/-14\%$). In the example of Figure 4, this may cause ± 800
picoseconds of phase shift between ϕ_{Ht} and ϕ_{Lt} as indicated by the filled portions 70 of the
timing diagrams.

Referring again to Figure 1, these variations in the two supply voltages may cause an out
25 of phase relationship between the clock signals 26 and 28 for circuit A 30 and circuit B 32. As
represented by line 48 in Figure 1, circuits 30 and 32 typically send signals to one another (e.g.,
when a register in circuit A 30 sends a signal to a register in circuit B 32). Depending upon the
particular application, these signals may be referenced to the master clock 44. Given that the
amount of the delay through the clock trees 40 and 42 may be dependent on supply voltage, it is
30 possible that there will be a phase difference (mismatch) between these clock signals.

This phase difference could have an adverse effect on data transfers between the two
circuits. For example, the phase difference typically would reduce the cycle time for circuit
operations. That is, the circuits will have to be designed to provide more delay in the system
timing between operations than would otherwise be required. This in turn would decrease the
35 speed at which the circuits could operate. Moreover, this mismatch may lead to race conditions
between registers that are clocked by clock signals 26 and 28.

In accordance with the invention, this phase mismatch may be corrected by varying the
delay of one of the clock signals (e.g., ϕ_{Ht}) to compensate for the phase mismatch between the

1 clock signals. This delay is regulated to keep the phase difference between the two clock signals as close to zero as possible. Figure 1 describes one embodiment of such a circuit. In Figure 1 a signal comparator 22 (e.g., a phase detector) compares the clock signals at the ends of the two clock trees 40 and 42 to determine the phase difference between the clock signals 26 and 28.
 5 Depending on the result of the comparison, the signal comparator 22 sends compensation signals to the delay adjuster 24 to increase or decrease the delay of clock signal to clock tree 40.

Referring now to Figure 5, a preferred embodiment of an analog delay locked loop ("DLL") for performing phase detection and delay adjustment operations is shown in block diagram form. In a manner similar to that described above, a reference clock signal ϕ_{76} is used to generate clock signals ϕ_{H78} and ϕ_{L80} . The clock signal ϕ_{L80} is generated from ϕ_{76} via a level shift and via buffers that comprise the ϕ_{L} clock tree (not shown). The clock signal ϕ_{H78} is generated from ϕ_{76} via an adjustable delay buffer 82 and via buffers 84 and 86 that comprise the ϕ_{H} clock tree. Phase detectors 88 and 90 compare ϕ_{H78} and ϕ_{L80} and generate signals that control the delay of adjustable delay buffer 82.

15 The operation of the adjustable delay buffer 82 of Figure 5 will be discussed in conjunction with Figures 6 and 7. Figure 6 is a schematic diagram of one embodiment of the adjustable delay buffer 82 implemented in CMOS circuitry. The adjustable delay buffer has input "i" and output "o" and is controlled by bias voltages V_{BIASP} and V_{BIASN} that affect the charging and discharging current to an intermediate node of the adjustable delay buffer 82.

20 MOS transistors P4 104 and N1 106 form a basic inverter for buffering and inverting input 'i' 108 to generate 'ob' 110. Signal 'ob' 110 is inverted to produce the non-inverted output 'o' of the adjustable delay buffer. PMOS transistors P1 112, P2 114 and P3 116 control current flow for the rise time of the basic inverter. P2 114 supplies a constant current because it is always ON with a grounded gate, thus defining the maximum rise time for 'ob' 110 when P1 112 and P3 116 are both off. P1 112 is either OFF or ON depending on the state of the "resetb" signal and, when ON, provides an intermediate supply current to the inverter. In a preferred embodiment, the circuit is designed so that the current supplied when P1 112 and P2 114 are both on is in the middle of the regulation window that is covered by the adjustable delay buffer 82. P3 116 provides an adjustable current to the inverter depending on the value of V_{BIASP} . Preferably, the ON and OFF states of P1 112 and P3 116 are mutually exclusive.

30 Transistors N2 118, N3 120 and N4 122 operate in a similar way for controlling current flow for the falling edge of 'ob' 110. N3 120 sinks a constant current because it is always ON with its gate tied to a high voltage thereby defining the maximum fall time for 'ob' 110 when N2 118 and N4 122 are both off. N2 118 is either OFF or ON depending on the state of the "reset" signal (the compliment of resetb) and, when ON, provides an intermediate sinking current for the inverter. In a preferred embodiment, the circuit is designed so that the current sunk when N2 118 and N3 120 are both ON is in the middle of the regulation window that is covered by the adjustable delay buffer 82. N4 122 sinks an adjustable current to the inverter depending on the

1 value of V_{BIASN} . Preferably, the ON and OFF states of N2 118 and N4 122 are mutually exclusive.

Through the use of the constant current transistors P2 114 and N3 120 and the reset signals, the adjustable delay buffer may be set to a maximum delay state or to a fixed
5 intermediate delay state. In practice, the transistors P1 112 and N2 118 are dimensioned so that under typical operating conditions, the buffer provides enough delay so that the output of the two clock trees are aligned in phase.

Adjustable delay is provided by varying V_{BIASP} and V_{BIASN} . As these signals are varied, the rise time and fall time of the inverter is varied resulting in a variable delay between 'i' 108
10 and 'ob' 110.

Figure 7 is a graph representative of delay adjustments for the adjustable delay buffer 82 of Figure 6. The vertical axis represents the rise times and fall times at "ob" 110. The horizontal axis represents the bias voltages V_{BIASP} and V_{BIASN} . V_{TN} is the threshold voltage of an NFET. V_{TP} is the threshold voltage of a PFET. In this example, the reset signals are inactive.

15 Curve $tf(ob)$ 126 corresponds to V_{BIASN} . When V_{BIASN} is below V_{TN} then the buffer 82 provides a constant delay for the falling edge because transistor N4 122 is off. As V_{BIASN} increases to values above V_{TN} N4 122 turns on thereby providing more sink current for N1 106. As a result, the fall time of node "ob" 110 decreases.

Curve $tr(ob)$ 128 corresponds to V_{BIASP} . When V_{BIASP} is above $V_{DD} - V_{TP}$ then the buffer
20 82 provides a constant delay for the rising edge because transistor P3 116 is off. As V_{BIASP} decreases to values below $V_{DD} - V_{TP}$ P3 116 turns on thereby providing more source current for P4 104. As a result, the rise time of node "ob" 110 decreases.

Figures 8A - 8D depict simulation results for the delays under typical conditions. Figure 8A illustrates the delay for the rising edge. Figure 8B illustrates the delay sensitivity (i.e., the
25 gradient of the delay curve: gradient delay over gradient bias voltage) for the rising edge. Figure 8C illustrates the delay for the falling edge. Figure 8D illustrates the delay sensitivity for the falling edge.

Referring again to Figure 5, the generation of V_{BIASP} and V_{BIASN} will be treated in detail. The phi signal 76 is fed through the adjustable delay buffer 82 and then through buffers 84 and
30 86 to generate ϕ_{iH} 78. The signal ϕ_{iH} 78 is used to clock the two phase detectors PDTF1 88 (clocked on the falling edge of ϕ_{iH}) and PDTR2 90 (clocked on the rising edge of ϕ_{iH}). The signal ϕ_{iL} 80 is used as the data signal to both of the phase detectors PDTF1 88 and PDTR2 90.

The phase detector for the falling edge, PDTF1 88, generates a control signal (early) which is one of two inputs to a nand gate 140. The resetb signal is the other input to the nand gate 140.
35 The digital output of nand gate 140 is fed to a low pass filter (consisting of R1 142 and C1 144) to generate the V_{BIASP} signal as an analog value.

Typically, the output of the nand gate 140 may remain high for a few clock cycles. This will cause V_{BIASP} to rise slowly. When the phase detector 88 detects that the falling edge of clock

1 signal ϕ_{iH} is no longer earlier than the input signal ϕ_{iL} , the phase detector 88 switches the early signal to its opposite value. At this point, the output of the nand gate 140 will go low. When this happens, V_{BIASP} will fall slowly. Thus, the value of V_{BIASP} will vary back and forth in relatively small intervals. The nand gate 140 functions to keep the ON and OFF state of the transistors P1 112 and P3 116 in Figure 6 mutually exclusive.

5 V_{BIASN} is generated in a similar fashion using the rising edge phase detector PDTR2 90 to control a nor gate 146 and the low pass filter consisting of resistor R2 148 and capacitor C2 150. The phase detector for the rising edge, PDTR2 90, generates a control signal (late) which is one of two inputs to nor gate 146. The resetb signal is the other input to the nor gate 146. The digital output of NOR gate 146 is fed to a low pass filter (consisting of R2 148 and C2 150) to generate the V_{BIASN} signal as an analog value.

10 Typically, the output of the nor gate 146 may remain high for a few clock cycles. This will cause V_{BIASN} to rise slowly. When the phase detector 90 detects that the rising edge clock signal ϕ_{iH} is no longer later than the input signal ϕ_{iL} , the phase detector 90 switches the late signal to its opposite value. At this point, the output of the nor gate 146 will go low. When this happens, V_{BIASN} will fall slowly. Thus, the value of V_{BIASN} will vary back and forth in relatively small intervals. The nor gate 146 functions to keep the ON and OFF state of the transistors N2 118 and N4 122 in Figure 6 mutually exclusive.

15 Figures 9 and 10 are circuit diagrams of one embodiment of the phase detectors 90 and 88 for the rising edge and the falling edge, respectively. Referring to Figure 9, this register circuit generates the late signal when ϕ_{iH} rises before ϕ_{iL} . Transistors P2 154 and N1 156 and transistors P3 158 and N2 160 form the sampling latch in the register. Transistor N3 163 is used to latch the state of the clock signal ϕ_{iL} when ϕ_{iH} is rising. Depending on which clock signal transitions first, the complementary latch outputs q 164 and qn 166 will be at a 1 or a 0 state, respectively.

20 Switch transistors 168 and 170 and the two inverters 172 and 174 form the output latch in the register. Because the latch is pre-charged, the pre-charge state could potentially become the output. To avoid this, the output (qn) 166 is latched into the output latch to generate the "late" signal. When the latch is precharging, the connection through the output latch is, in effect, broken so that the output latch stores the value of the previous evaluation by the sampling latch, not the precharge value. The inverter 176 is used to provide the same load on output q 164 as is present on output qn 166.

25 Referring now to the falling edge detector 88 in Figure 10, this register circuit generates the early signal when ϕ_{iL} falls before ϕ_{iH} . Transistors P2 180 and N2 182 and transistors P3 184 and N3 186 form the sampling latch in the register. Transistor P1 189 is used to latch the state of ϕ_{iL} when ϕ_{iH} is falling. Depending on which clock signal transitions first, the complementary latch outputs q 192 and qn 194 will be at a 1 or a 0 state, respectively.

30 Switch transistors 196 and 198 and the two inverters 200 and 202 form the output latch

1 in the register for reasons similar to those discussed above in conjunction with Figure 9. Similarly, inverter 204 is used to provide the same load on output q 192 as is present on output qn 194.

5 Figure 11 shows an exemplary implementation for the low pass filters R1 142 and C1 144 and R2 148 and C2 150, using CMOS technology. That is, the circuits on the right side of Figure 11 are the CMOS implementations of the RC circuits depicted on the left side of Figure 11.

Figure 12 depicts a delay measurement ($\Delta\tau_H$) for an exemplary analog DLL where there is a mismatch between the delay for ϕ_H and ϕ_L . In operation, the analog DLL described herein will adjust τ_H to match τ_L ($\Delta\tau_H = 0$). It will be understood by those skilled in the art that the accuracy with which the analog DLL can match τ_H to τ_L depends on a variety of factors including, for example, circuit characteristics, operating condition and manufacturing tolerances. In general, while the goal is to obtain a perfect match at all times between τ_H and τ_L , in practice this match will be somewhat less than exact.

15 Figures 13A - 13E show simulation results for different states of an exemplary analog DLL. Figure 13A depicts a buffer mismatch (the values of $\Delta\tau_H$ for several corner conditions) when reset is set to a "1." Figure 13B depicts a buffer mismatch when reset is set to a "0." These simulations illustrate the circuit of Figure 5 reduces clock uncertainty by a factor of three. Figure 13C depicts buffer mismatch hysteresis for several corner conditions when reset is set to a "0." Figure 13D depicts tracking range under the conditions $V_{DDH} = 2.5V$, $V_{DDL} = 1.8V$ at corner TT and a temperature of 25 °C. Figure 13D depicts tracking hysteresis under the conditions $V_{DDH} = 2.5V$, $V_{DDL} = 1.8V$ at corner TT and a temperature of 25 °C.

Referring now to Figure 14, this figure describes another embodiment of the invention wherein a digital delay locked loop ("DLL") is used to compensate for the phase variations of two clocks, ϕ_H and ϕ_L . In this circuit, several delay elements, e.g., buffers 210, 212, 214, 216 and 218, are used to generate delayed versions of the input clock signal ϕ . A delay selector comprising selector switch 222 and counter1 230 selects the one delayed clock signal that provides the best match to the desired phase of the output clock. In other words, selector switch 222 controls the delay of ϕ_H to match the phase of ϕ_L by selecting a version of the clock signal ϕ that has passed through as few as none (switch 222 connects output lead 234 to input lead 236) and as many as five (switch 222 connects output lead 234 to input lead 238) of the buffers 210 - 218. Flip-flop DFF1 224 performs the function of a phase detector. Flop-flops DFF2 226 and DFF3 228 are signal stabilizers that help resolve meta stability conditions that exist due to the circuit driving DFF1 224 so that ϕ_H clocks the DFF1 224 when ϕ_L is in transition. Counter1 230 controls the position of the selector switch 222 based on the phase difference between ϕ_H and ϕ_L . Counter2 232 is, in effect, a low pass filter that reduces jitter in the circuit so that the jitter does not effect the position of the selector switch 222.

Basically, each transition of the clock signal output is a phase measurement and this results in a high or low output by DFF3 228 that feeds to counter1 230 through the low pass filter

1 (counter2 232). When the phases of the ϕ_{H} and ϕ_{L} are equal, the output of DFF3 228 will toggle thereby setting counter2 232 to alternate between counting up and counting down. In this case, the output of counter2 will not saturate in either the high or low direction. As a result, counter1 230 will not change the position of the selector switch 222. In the event of a phase mismatch between ϕ_{H} and ϕ_{L} , counter2 232 may eventually saturate (high or low) at some defined value which will cause counter1 230 to change the position of the selector switch 222.

The minimum resolution of this digital delay lock loop is limited to the delay of one buffer. In practice, this resolution may be too large to provide adequate delay compensation in certain circuits.

10 Figure 15 is a block diagram of an alternative embodiment of a circuit for implementing a variable delay in a digital scheme. For example, the circuit of Figure 15 could replace the buffers 210 - 218 and the selector switch 222 of Figure 14. The delay in this circuit is controlled by selecting the path of the input signal ϕ through delay elements consisting of multiplexors ("Muxs") 240, 242, 244 and 246 and inverters 248, 250, 252, 254 and 256. Muxs 240, 242, 244 and 246 may, in general, be selected by the output of counter1 in Figure 14 (e.g., using a thermometer code). The next shortest signal path through this structure is through Mux0 240. The next selection has a delay that results from propagation through inverter 248, Mux1 242 and Mux0 240. Therefore, incremental delays can be added by going one step to the right through an additional inverter and the corresponding Mux delay. The advantage of this structure is that the select switch does not have to be balanced as it typically would be in the embodiment of Figure 14. When the signal is switched from one path to the next path, only an inverter and a Mux delay are added.

The digital delay locked loop has several advantages over the analog delay locked loop. For example, the digital embodiments may be easier to implement than the analog embodiments because a digital circuit may be constructed using gates from a standard cell library. Moreover, the parameters of the digital circuit are relatively stable; whereas the parameters of, for example, the low pass filter in the analog circuit may change depending on the process corner of the chip, the particular lot of the chip and operating conditions such as temperature and supply voltage.

25 However, the minimum resolution of the digital circuit typically is limited to the delay of a Mux plus an inverter. For example, in one embodiment, with operating conditions of $V_{DD} = 2.5V$, SS corner, temperature = 25 °C, the delay is quantized to approximately 0.35 nS. Thus, the delay is slightly longer than the one buffer delay described in conjunction with Figure 14.

30 In one embodiment, the phase error between ϕ_{H} and ϕ_{L} is approximately +/-400 picoseconds ("pS") with changes in V_{DD} of +/-10%. The phase error is approximately +/-200 pS with changes in V_{DD} of +/-5%. Thus, the resolution of the embodiments of the digital DLL described above is not small enough to provide effective delay compensation in this case. In sum, for practical application of the digital DLL, it is important to select delay components that have sufficiently small delay, e.g., appreciably smaller than the maximum phase error between

1 ϕ_{H} and ϕ_{L} .

 A comparison of the analog DLL and the digital DLLs described above illustrate that the analog DLL may be preferable to the digital DLL in many circumstances. For example an analog DLL that aligns the rising and falling edges is preferable to a digital design that aligns only one
5 edge (e.g., the rising edge). Clock jitter (e.g., τ_{hyst}) in one embodiment of the analog DLL is approximately 0.06 nS. In one of the digital embodiments, the clock jitter was approximately 0.35 nS. Also, in the digital DLL delay is quantized (e.g., 0.35 nS) while the analog DLL can, in effect, continuously track changes in the delay. In addition, the digital DLL may consume more power than the analog DLL due to switching activity that may occur in digital DLL
10 implementations. In sum, the analog DLL may provide better performance at a lower cost.

 Referring to Figure 16, in one embodiment a circuit constructed according to the invention is implemented as an integrated circuit-based bidirectional communication system. In this case, the present invention may be characterized as a system and method for accommodating efficient, high speed decoding of signal samples encoded according to the trellis code specified in the IEEE
15 802.3ab standard (also termed 1000BASE-T standard). The physical implementation of this embodiment is a gigabit ethernet transceiver chip 266 that is installed on a transceiver circuit board 268. The decoder circuitry portions of transceiver demodulation blocks require a multiplicity of operational steps to be taken in order to effectively decode each symbol. Such a multiplicity of operations is computationally complex and may push the switching speeds of
20 integrated circuit transistors which make up the computational blocks to their fundamental limits. Consequently, the transceiver chip 266 may use multiple supply voltages to reduce the power dissipation of the integrated circuit.

 Figure 17 is a simplified block diagram of the functional architecture and internal construction of the transceiver chip 266 and other portions of the transceiver board 268. In one
25 embodiment of this implementation, circuits such as echo canceller 260 and near-end crosstalk ("NEXT") cancellers 262 may be operated at a lower supply voltage than some of the other circuits in the transceiver chip. In this case, a lower supply voltage powers the components that generate the clock signals for clocking the Echo/NEXT cancellers. In accordance with the invention, a clock circuit (not shown) may incorporate phase compensation to reduce phase
30 mismatches between the clocks sent to the echo cancellers 260 and the NEXT cancellers 262 and the clocks sent to other circuits in the transceiver chip 266.

 Figure 18 is a simplified block diagram of some of the trellis decode functionality from decode block 270 in the transceiver chip 266. The decode functionality includes a decision feedback equalizer 264 ("DFE") that may be operated at a lower supply voltage than some of the
35 other circuits in the transceiver chip 266. In this case, a lower supply voltage powers the components that generate the clock signals for clocking the DFE 264. As discussed above, the timing recovery circuit 258 may incorporate phase compensation to reduce phase mismatches between the clocks sent to the DFE 264 and the clocks sent to other circuits in the transceiver

1 chip 266.

2 In summary, the invention described herein provides an effective technique for
3 compensating for phase mismatches that may occur as a result of variations in power supply
4 outputs. While certain exemplary embodiments have been described in detail and shown in the
5 accompanying drawings, it is to be understood that such embodiments are merely illustrative of
6 and not restrictive of the broad invention. It will thus be recognized that various modifications
7 may be made to the illustrated and other embodiments of the invention described above, without
8 departing from the broad inventive scope thereof.

9 For example, a variety of circuits may be used to implement analog DLLs and digital
10 DLLs in accordance with the invention. The invention may be embodied in many different
11 forms, for example, in virtually any type of integrated circuit. That is, the teachings of the
12 invention are not limited to any particular integrated circuit function or structure. Moreover, such
13 an integrated circuit could be used in a variety of devices such as transceiver boards 268 in
14 personal computers, network interface cards and network infrastructure switches. It should be
15 understood by one skilled in the art, given the teachings of the invention, that the operating
16 characteristics of the analog and digital DLLs will depend, for example, on circuit parameters and
17 operating conditions.

18 In addition, it would be apparent to one skilled in the art based on the description herein
19 that the teachings of the invention may be applied to circuits that incorporate any number of
20 supply voltages and signals (e.g., clock signals). For example, in the case where three supply
21 voltages are used in the system S of Figure 1, a third clock tree and level shifter (not shown)
22 could be used to supply the clock signals to a third circuit (e.g., circuit C, not shown). In
23 addition, another delay adjust circuit could be used in circuit B or C. In this case, the signal
24 comparator also would compare the output of the third clock tree to control the delay adjust
25 circuits so that the clocks for all three of the circuits are closely synchronized.

26 In view of the above it will be understood that the invention is not limited to the particular
27 embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations
28 or modifications which are within the scope and spirit of the invention as defined by the
29 appended claims.

1 WHAT IS CLAIMED IS:

1. A system for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising:
 - 5 at least one phase comparator for comparing a phase of a first signal associated with a first signal level with a phase of a second signal associated with a second signal level, and for generating at least one compensation signal indicative of a phase difference between the first signal and the second signal; and
 - at least one delay adjuster coupled to the at least one phase comparator and
10 responsive to the at least one compensation signal, for delaying the first signal to compensate for the phase difference between the first signal and the second signal.
2. The system of claim 1 wherein the at least one delay adjuster comprises at least one
15 adjustable delay buffer.
3. The system of claim 2 wherein the at least one phase comparator comprises:
 - a rising edge phase comparator for comparing a rising edge of the first signal with
a rising edge of the second signal, for generating at least one rising edge compensation
signal indicative of a phase difference between the rising edge of the first signal and the
20 rising edge of the second signal; and
 - a falling edge phase comparator for comparing a falling edge of the first signal with
a falling edge of the second signal, for generating at least one falling edge compensation
signal indicative of a phase difference between the falling edge of the first signal and the
falling edge of the second signal.
25
4. The system of claim 1 wherein the at least one adjustable delay buffer:
 - delays the rising edge of the first signal in response to the rising edge compensation
signal; and
 - delays the falling edge of the first signal in response to the falling edge
30 compensation signal.
5. The system of claim 2 wherein the at least one adjustable delay buffer comprises:
 - at least one buffer transistor for buffering the first signal; and
 - at least one control transistor, responsive to the at least one compensation signal,
35 for adjusting current flow through the at least one buffer transistor for controlling delay of the first signal through the at least one buffer transistor.

- 1 6. The system of claim 1 further comprising a plurality of buffers for generating the first
signal and the second signal.
7. The system of claim 6 wherein the plurality of buffers comprise a plurality of clock trees.
- 5 8. The system of claim 1 further comprising at least one power supply for providing a
plurality of supply voltages associated with the plurality of signal levels.
9. The system of claim 1 wherein the first signal and the second signal are derived from a
10 common clock signal.
10. A system for compensating for phase differences between a plurality of signals,
comprising:
- 15 a level adjuster for modifying a signal level of a signal to generate a first signal
associated with a first signal level that is different than a second signal level associated
with a second signal;
- at least one phase comparator for comparing a phase of the first signal with a phase
of the second signal, and for generating at least one compensation signal indicative of a
phase difference between the first signal and the second signal ; and
- 20 at least one delay adjuster coupled to the at least one phase comparator and
responsive to the at least one compensation signal, for delaying at least one of the first
signal and the second signal to compensate for the phase difference between the first
signal and the second signal.
- 25 11. The system of claim 10 wherein the at least one delay adjuster comprises at least one
adjustable delay buffer.
12. The system of claim 11 wherein the at least one phase comparator comprises:
- 30 a rising edge phase comparator for comparing a rising edge of the first signal with
a rising edge of the second signal, for generating at least one rising edge compensation
signal indicative of a phase difference between the rising edge of the first signal and the
rising edge of the second signal; and
- a falling edge phase comparator for comparing a falling edge of the first signal with
a falling edge of the second signal, for generating at least one falling edge compensation
35 signal indicative of a phase difference between the falling edge of the first signal and the
falling edge of the second signal.
13. The system of claim 12 wherein the at least one adjustable delay buffer :

1 delays the rising edge of at least one of the first signal and the second signal in
response to the rising edge compensation signal; and
 delays the falling edge of at least one of the first signal and the second signal in
response to the falling edge compensation signal.

5

14. The system of claim 11 wherein the at least one adjustable delay buffer comprises:
 at least one buffer transistor for buffering the first signal; and
 at least one control transistor, responsive to the at least one compensation signal,
for adjusting current flow through the at least one buffer transistor for controlling delay
10 of the first signal through the at least one buffer transistor.

10

15. An integrated circuit including circuitry for compensating for phase differences between
a plurality of clock signals, comprising:

 a level adjuster for modifying a signal level of a signal to generate a first signal
15 associated with a first signal level that is different than a second signal level associated
with a second signal;

15

 at least one phase comparator for comparing a phase of the first signal with a phase
of the second signal, and for generating at least one compensation signal indicative of a
phase difference between the first signal and the second signal ; and

20 at least one delay adjuster coupled to the at least one phase comparator and
responsive to the at least one compensation signal, for delaying at least one of the first
signal and the second signal to compensate for the phase difference between the first
signal and the second signal.

20

25 16. The integrated circuit of claim 15 wherein the integrated circuit comprises an gigabit
ethernet transceiver.

25

17. The integrated circuit of claim 16 wherein the first signal comprises a clock signal that is
associated with at least one of a near end crosstalk canceller, an echo canceller and a decision
30 feed back equalizer.

30

18. A circuit for compensating for phase differences between a plurality of signals associated
with a plurality of signal levels, comprising:

 a rising edge phase comparator for comparing a rising edge of a first signal associated with
35 a first signal level with a rising edge of a second signal associated with a second signal level, for
generating a rising edge compensation signal indicative of a phase difference between the rising
edge of the first signal and the rising edge of the second signal;

35

 a falling edge phase comparator for comparing a falling edge of the first signal with a

1 falling edge of the second signal, for generating a falling edge compensation signal indicative of
a phase difference between the falling edge of the first signal and the falling edge of the second
signal; and

5 an adjustable delay buffer coupled to the rising edge comparator and the falling edge
comparator, for delaying the rising edge of the first signal in response to the rising edge
compensation signal and for delaying the falling edge of the first signal in response to the falling
edge compensation signal.

10 19. The circuit of claim 18 wherein the adjustable delay buffer comprises:

at least one buffer transistor for buffering the first signal;

at least one rising edge control transistor, responsive to the rising edge
compensation signal, for adjusting current flow through the at least one buffer transistor
for controlling delay of the rising edge of the first signal through the at least one buffer
transistor; and

15 at least one falling edge control transistor, responsive to the falling edge
compensation signal, for adjusting current flow through the at least one buffer transistor
for controlling the delay of the falling edge of the first signal through the at least one
buffer transistor.

20 20. The circuit of claim 19 wherein:

the rising edge phase comparator comprises a register for determining whether the
rising edge of the first signal leads the rising edge of the second signal; and

the falling edge phase comparator comprises a register for determining whether the
falling edge of the second signal leads the falling edge of the first signal.

25 21. The circuit of claim 20 further comprising a plurality of low pass filters for filtering the
rising edge compensation signal and the falling edge compensation signal.

30 22. A circuit for compensating for phase differences between a plurality of signals associated
with a plurality of signal levels, comprising:

at least one phase comparator for comparing a phase of a first signal associated with a first
signal level with a phase of a second signal associated with a second signal level, and for
generating at least one compensation signal indicative of a phase difference between the first
signal and the second signal;

35 a plurality of delay elements for selectively delaying the first signal; and

a delay selector coupled to the at least one comparator and responsive to the at least one
compensation signal, for selectively routing the first signal through at least one of the plurality

1 of delay elements to compensate for the phase difference between the first signal and the second
signal.

23. The circuit of claim 22 wherein the at least one phase comparator comprises at least one
5 flip-flop.

24. The circuit of claim 22 wherein the plurality of delay elements comprise a plurality of
buffers.

10 25. The circuit of claim 22 wherein the plurality of delay elements comprise a plurality of
multiplexers.

26. A method for compensating for phase differences between a plurality of signals associated
with a plurality of signal levels, comprising the steps of:

15 generating a first signal associated with a first signal level;
generating a second signal associated with a second signal level;
comparing a phase of the first signal with a phase of the second signal to generate
at least one compensation signal indicative of a phase difference between the first signal
and the second signal; and

20 delaying the first signal to compensate for the phase difference between the first
signal and the second signal.

27. The method of claim 26 wherein:

25 the comparing step further comprises the steps of:
comparing a rising edge of the first signal with a rising edge of the second
signal to generate a rising edge compensation signal indicative of a phase
difference between the rising edge of the first signal and the rising edge of the
second signal; and

30 comparing a falling edge of the first signal with a falling edge of the second
signal to generate a falling edge compensation signal indicative of a phase
difference between the falling edge of the first signal and the falling edge of the
second signal; and the delaying step further comprises the steps of:

delaying the rising edge of the first signal in response to the rising edge
compensation signal; and

35 delaying the falling edge of the first signal in response to the falling edge
compensation signal.

1 28. The method of claim 26 further comprising the step of selectively routing the first signal
through at least one of a plurality of delay elements to compensate for the phase difference
between the first signal and the second signal.

5 29. The method of claim 26 further comprising the steps of generating the first signal and the
second signal with a plurality of clock trees.

10

15

20

25

30

35

1/25

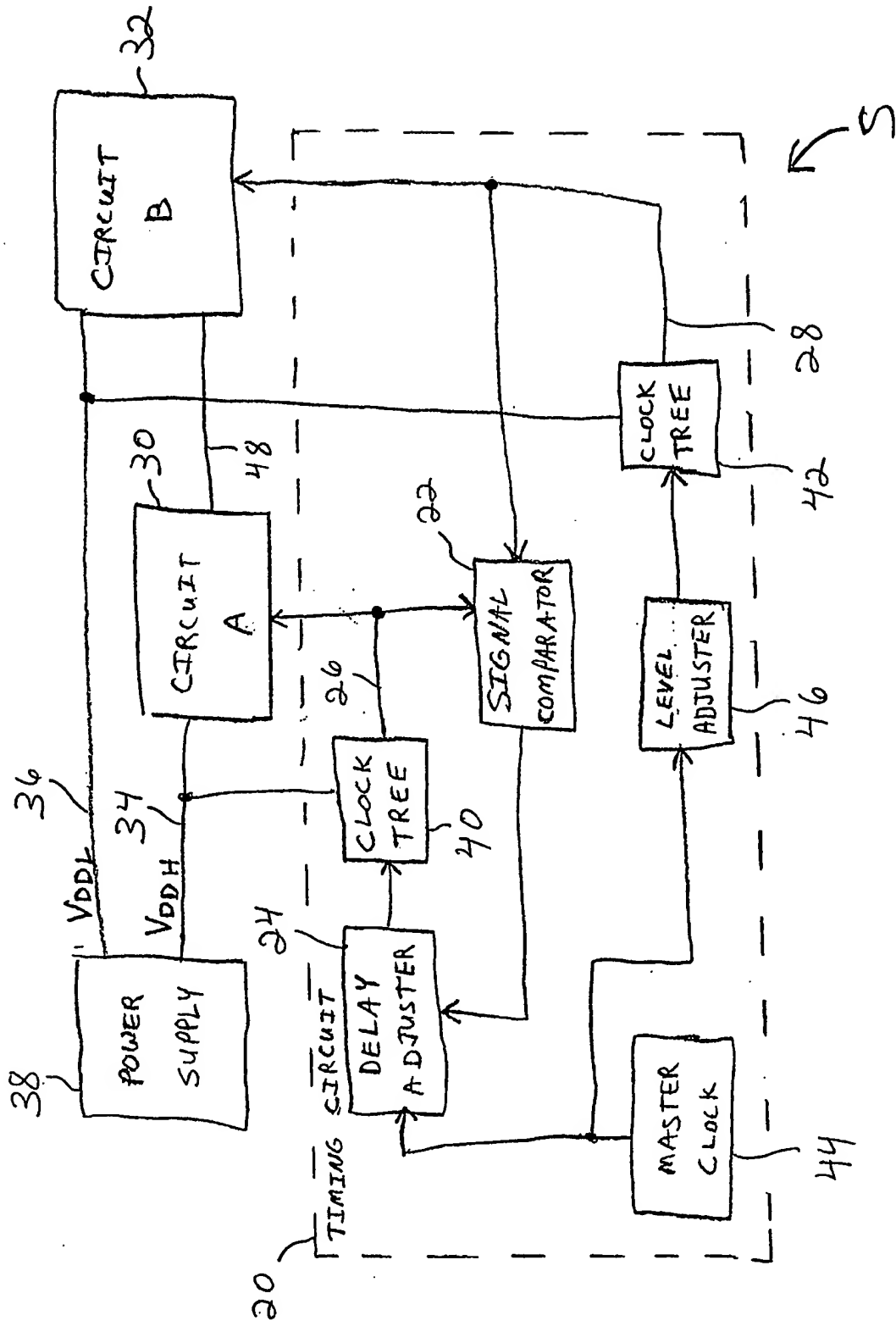


Fig. 1

2/25

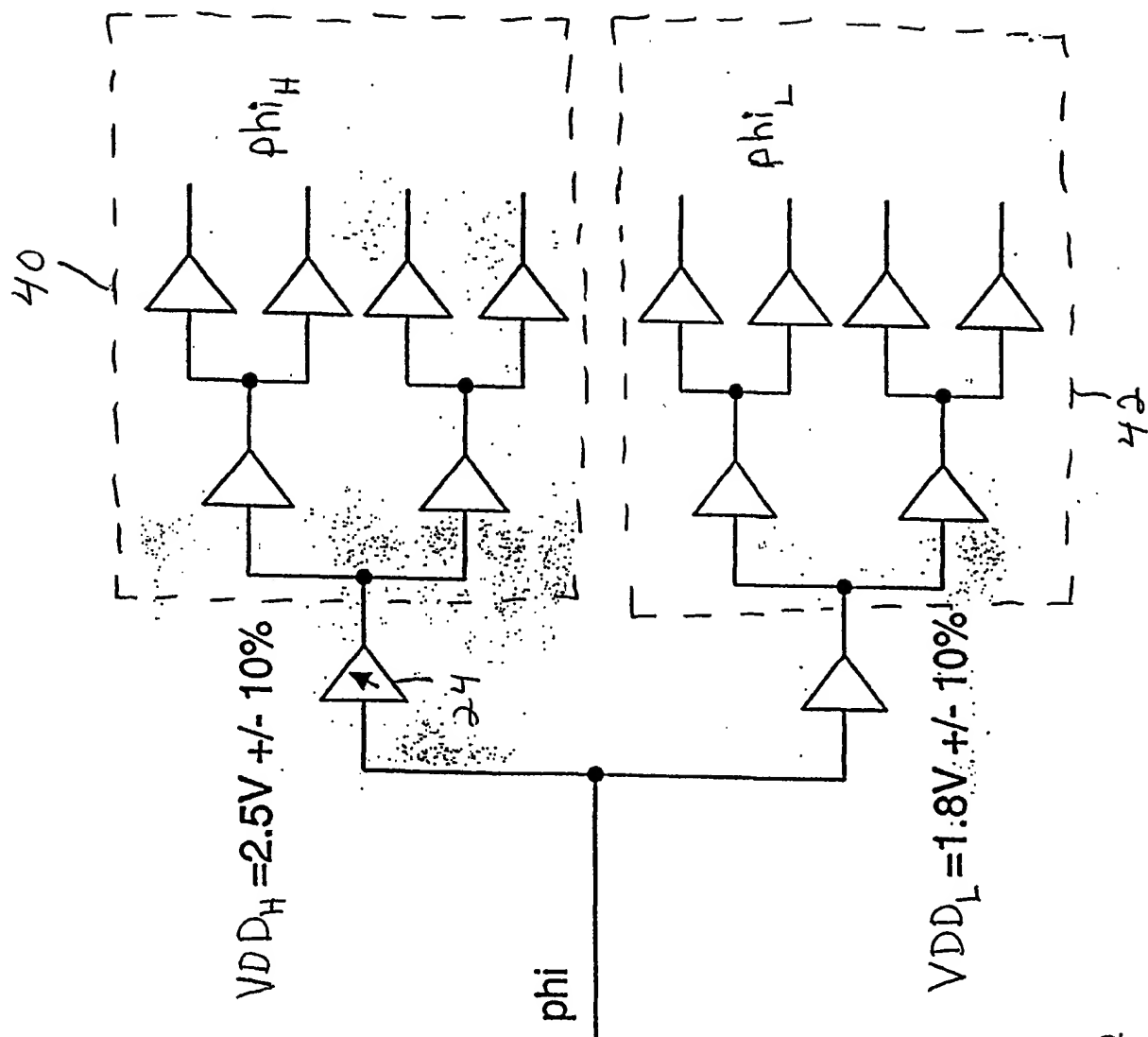
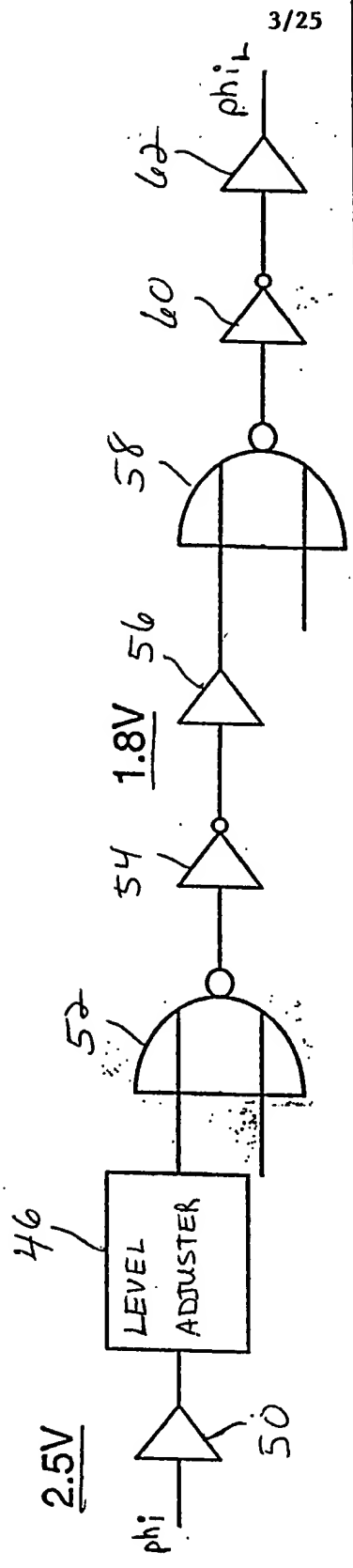


Fig. 2



3/25

Delay / ns		Σ	
SS	0.42	1.78	1.25
TT	0.26	1.02	0.72
FF	0.20	0.68	0.48
			3.45
			2.00
			1.36

Fig. 3

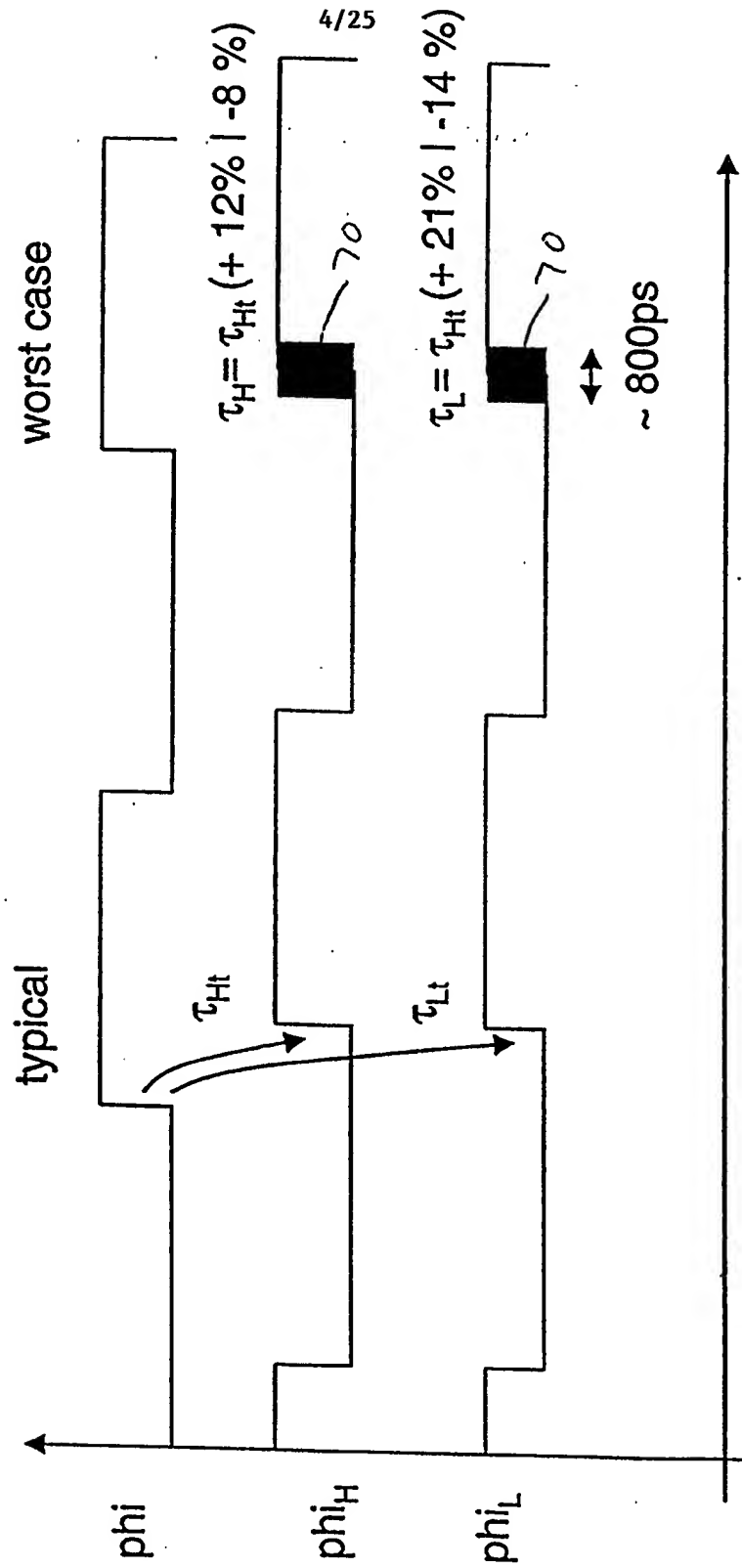


Fig. 4

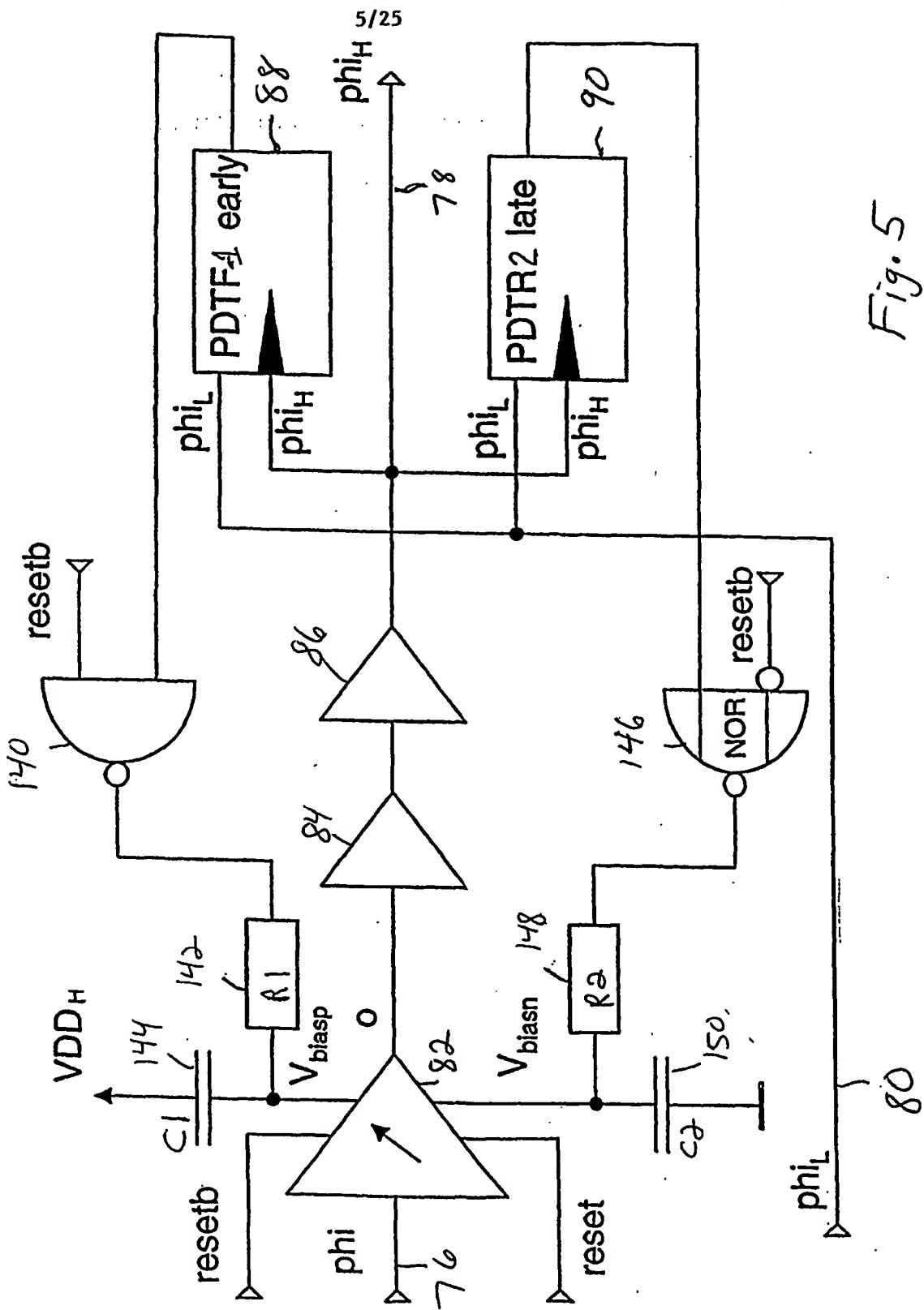
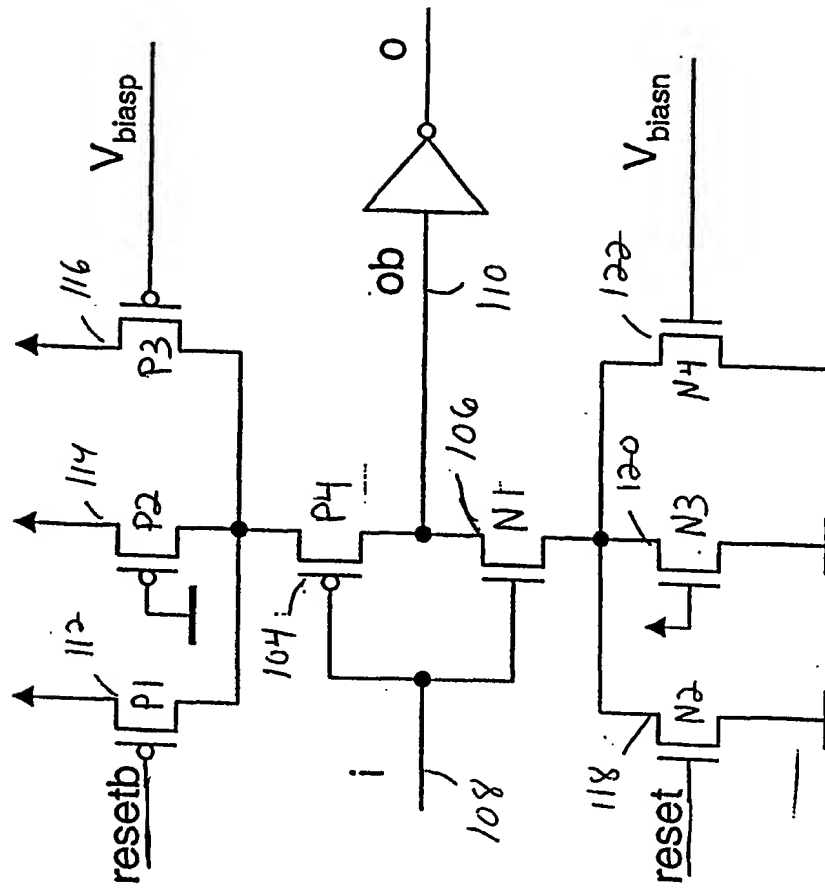


Fig. 5

6/25

82

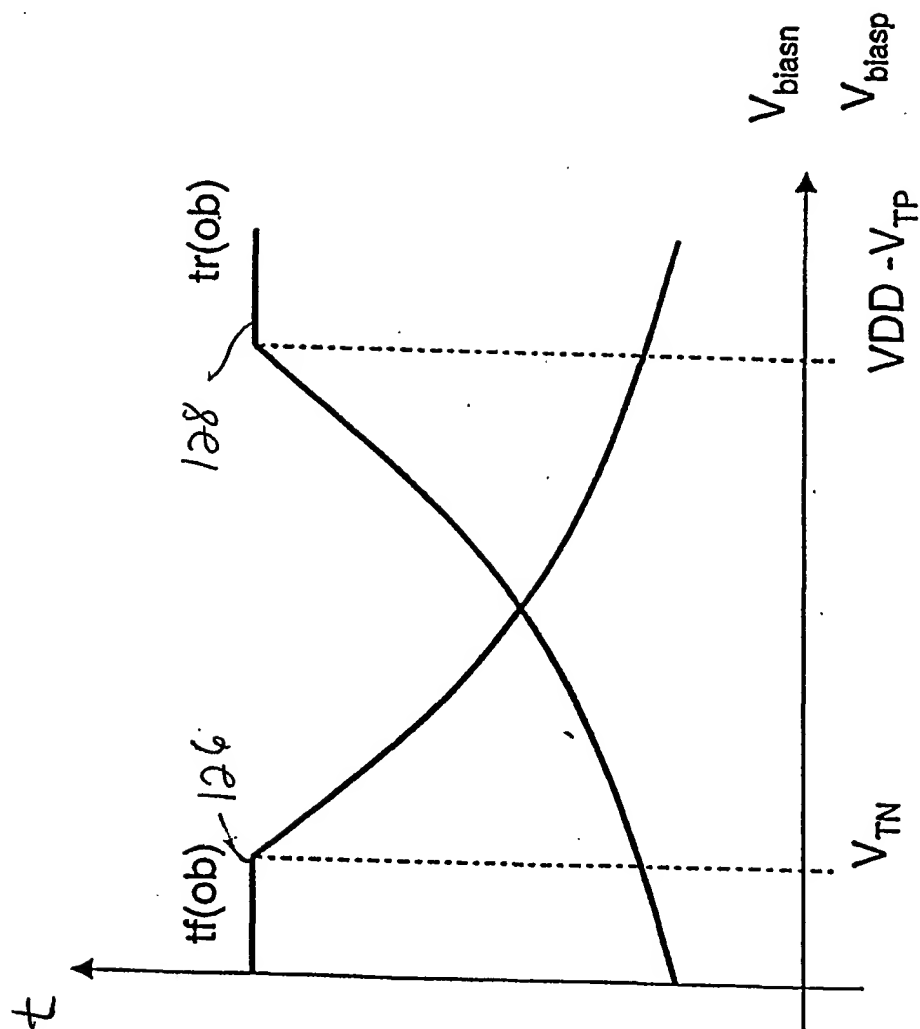
Fig. 4



7/25

tr: rise time
tf: fall time

Fig. 7



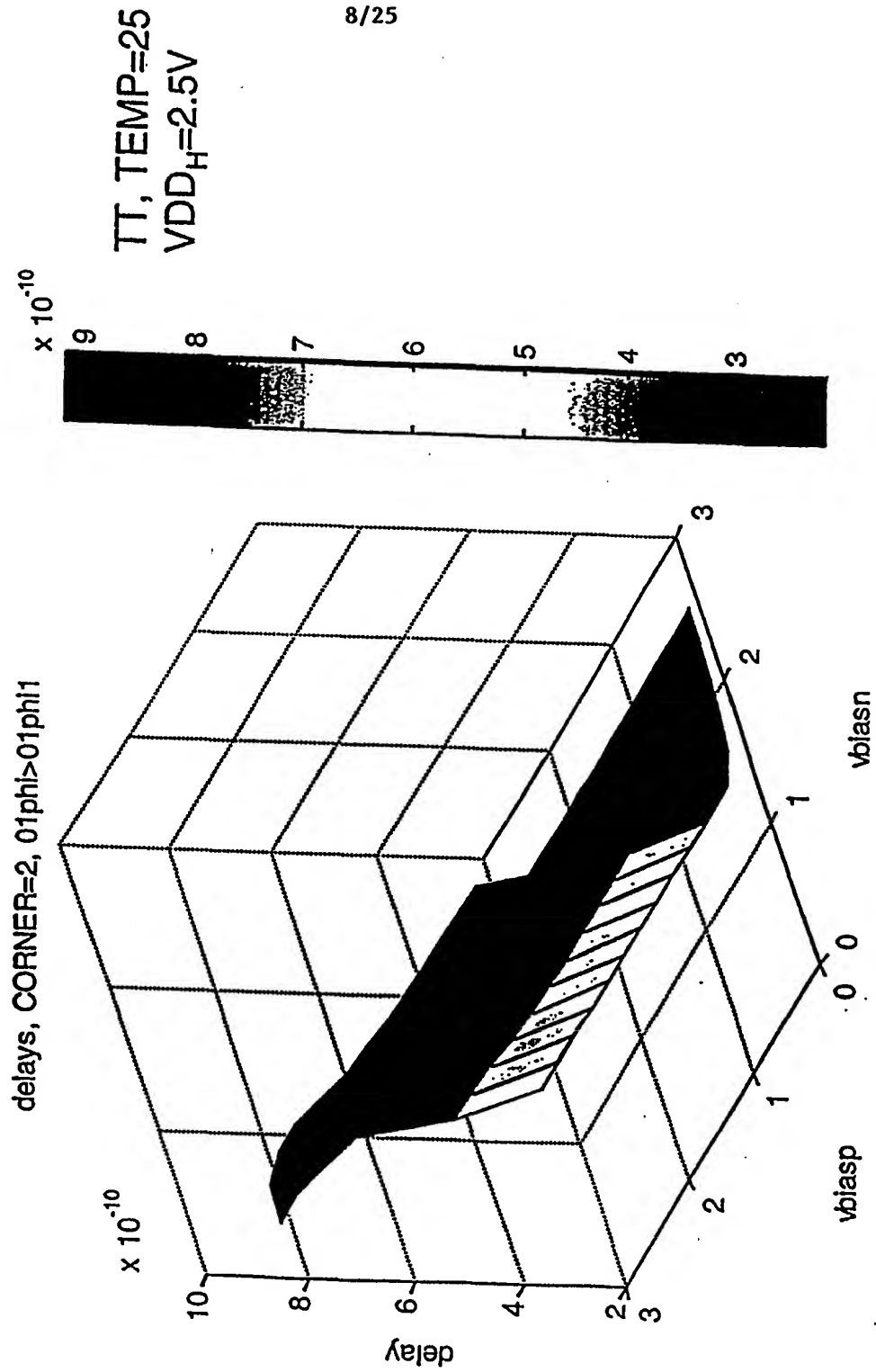


Fig. 8A

9/25

TT, TEMP=25
VDD_H=2.5V

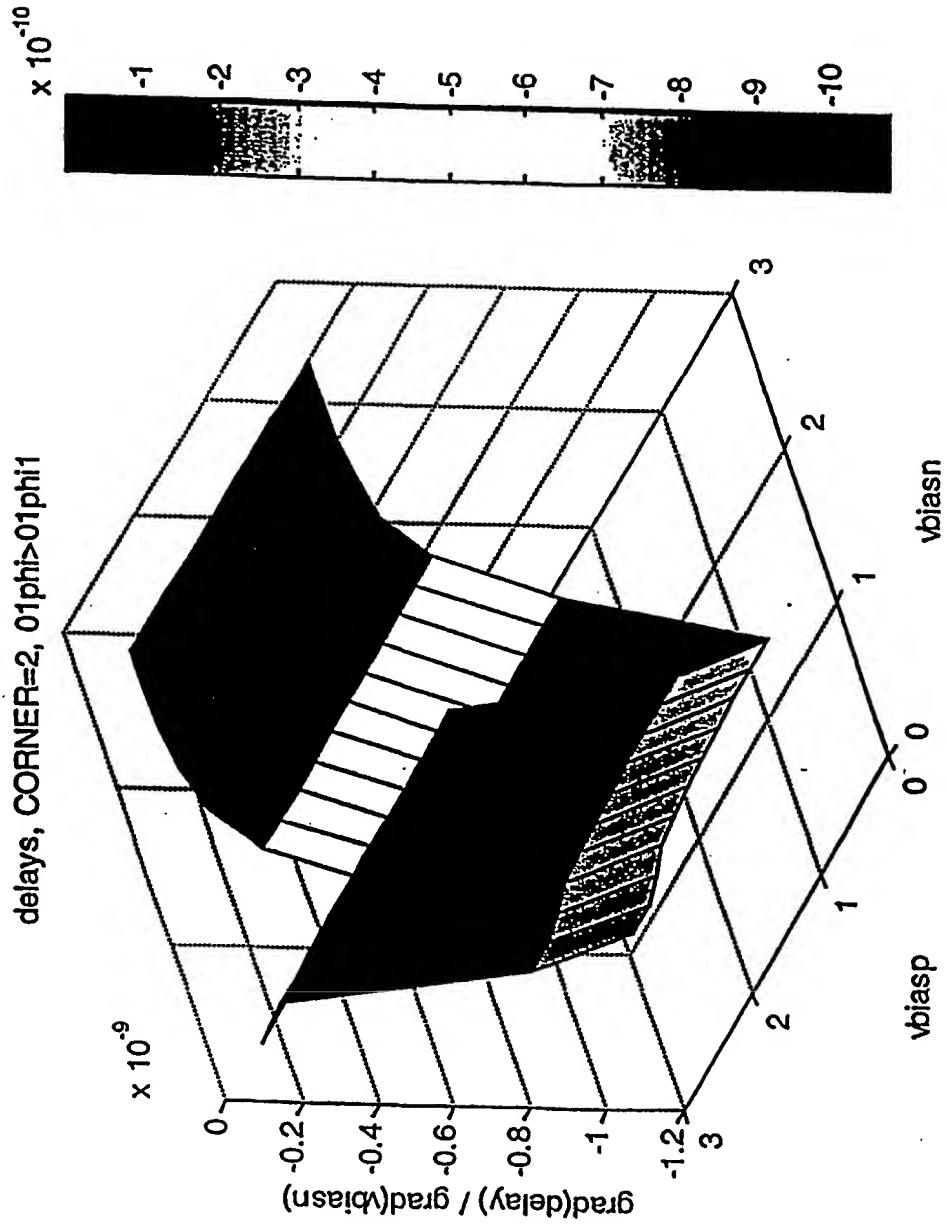


Fig. 8B

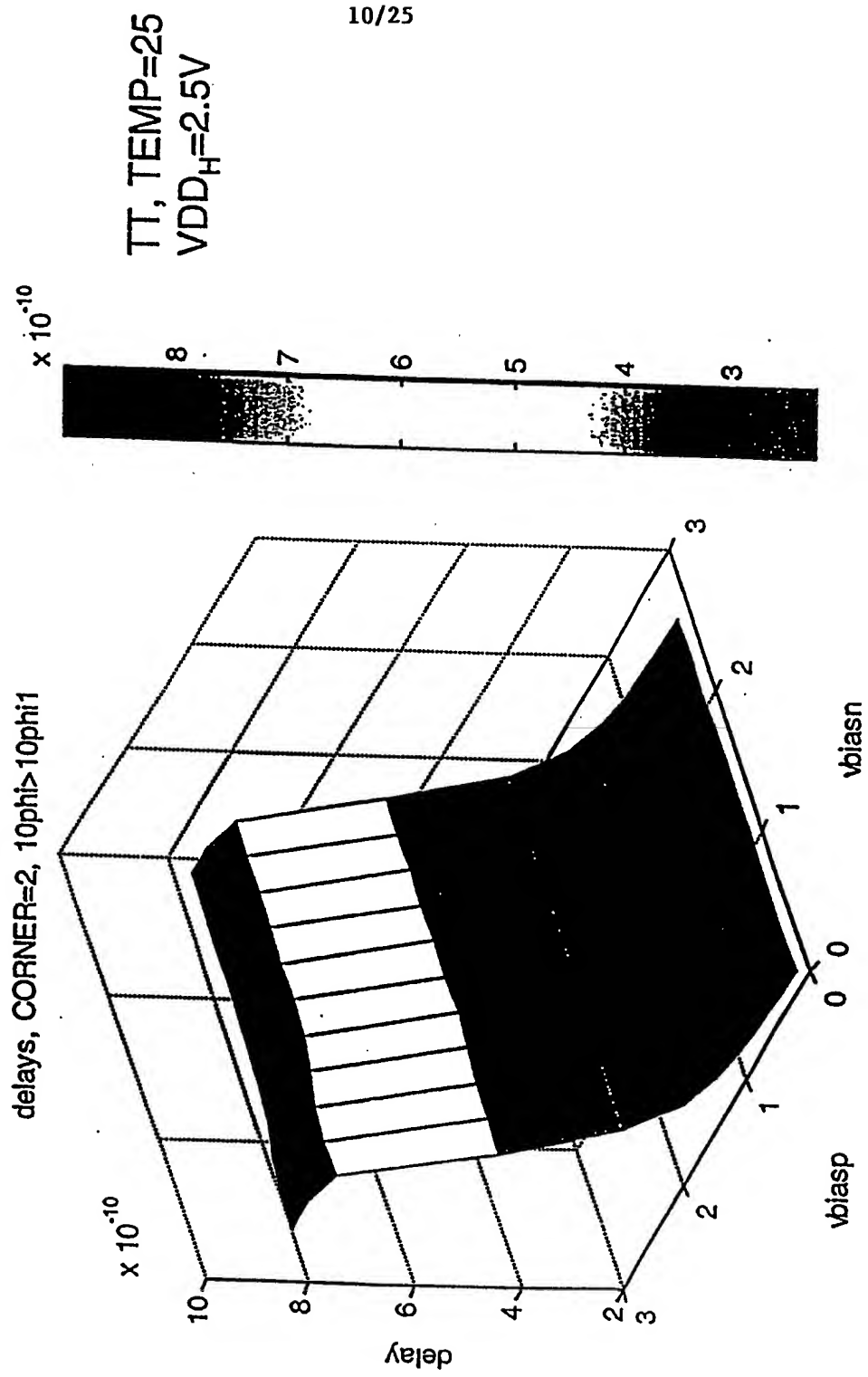


Fig. 8c

11/25

, TEMP=25
ID_H=2.5V

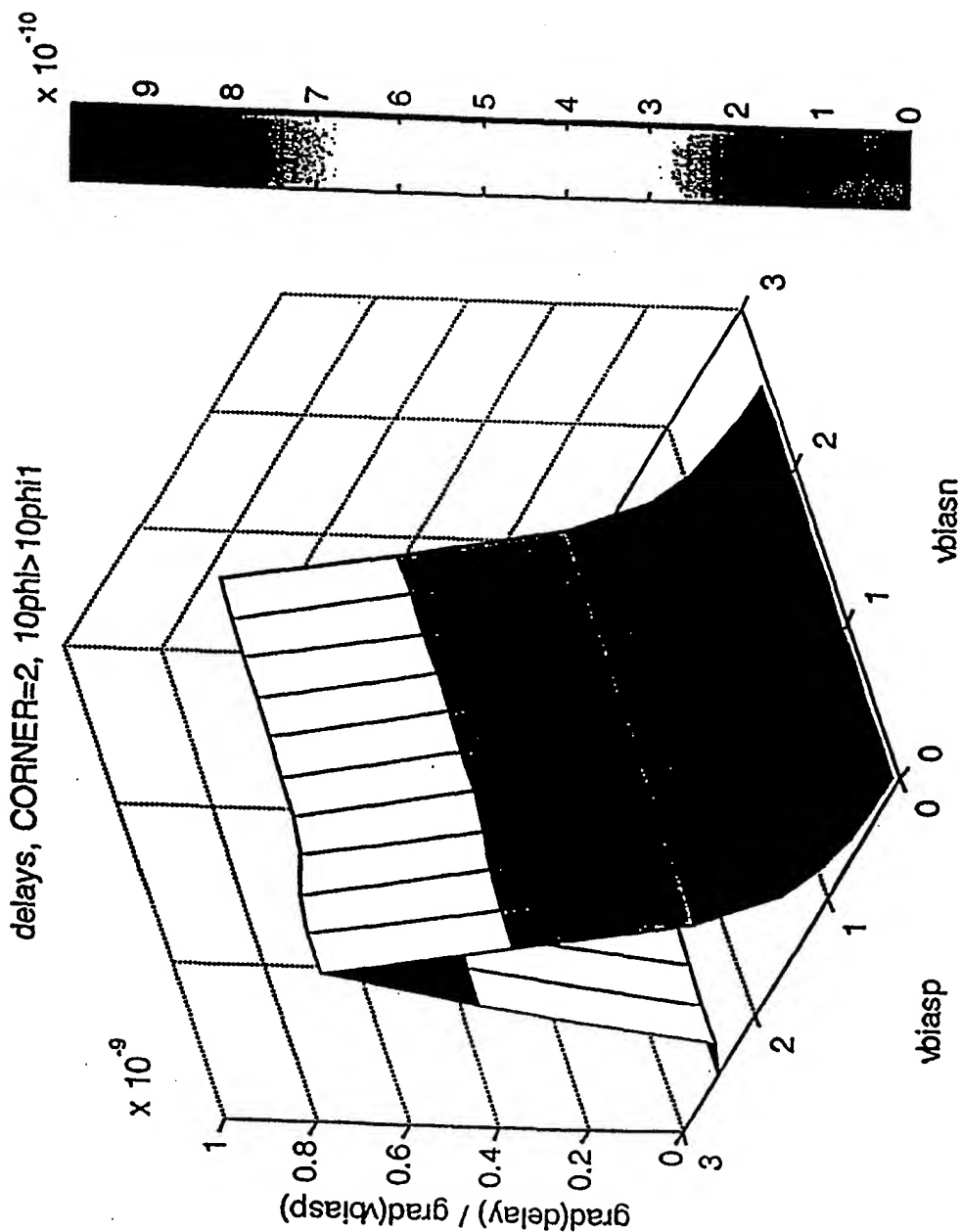


Fig. 8D

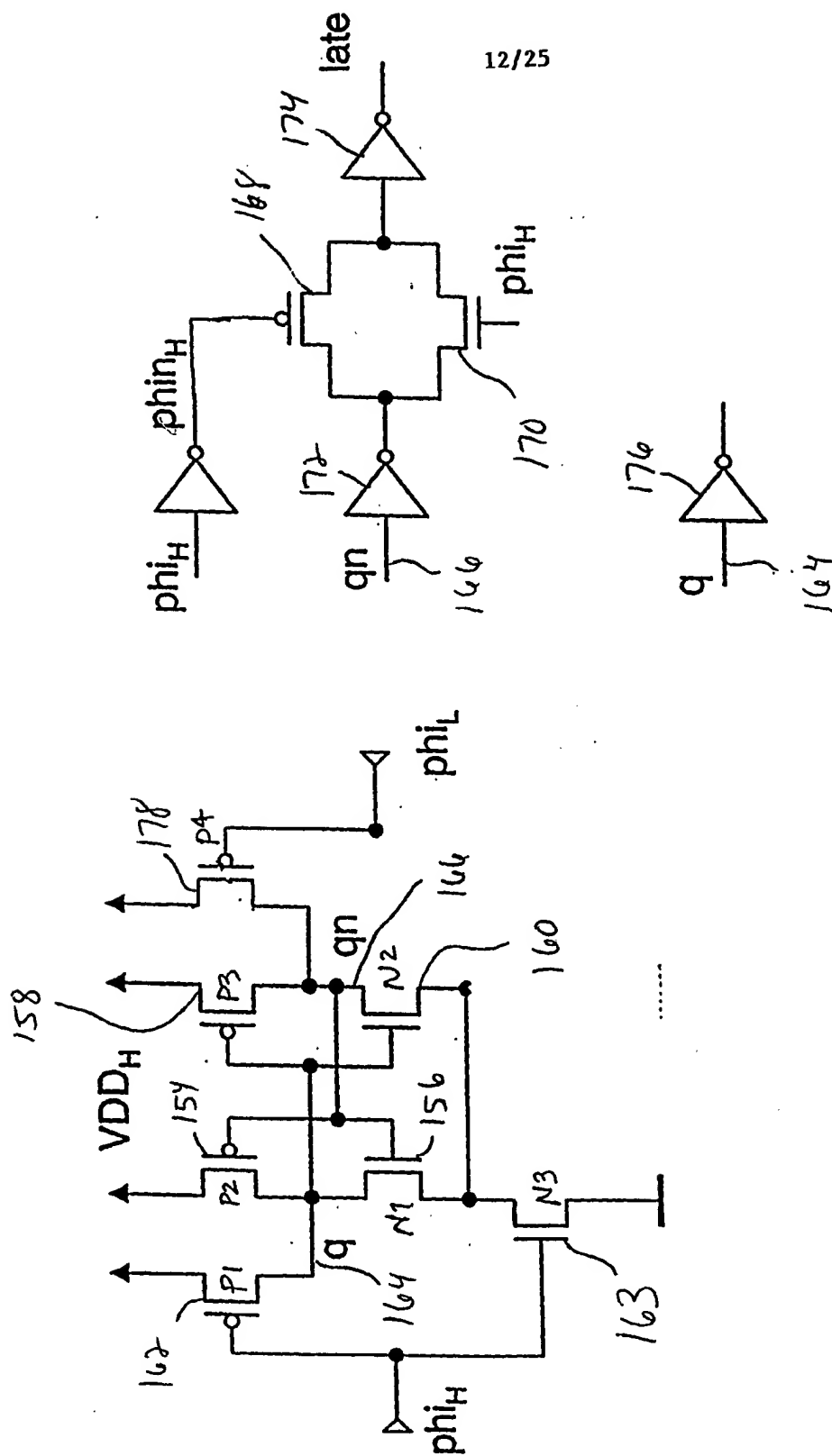


Fig. 9

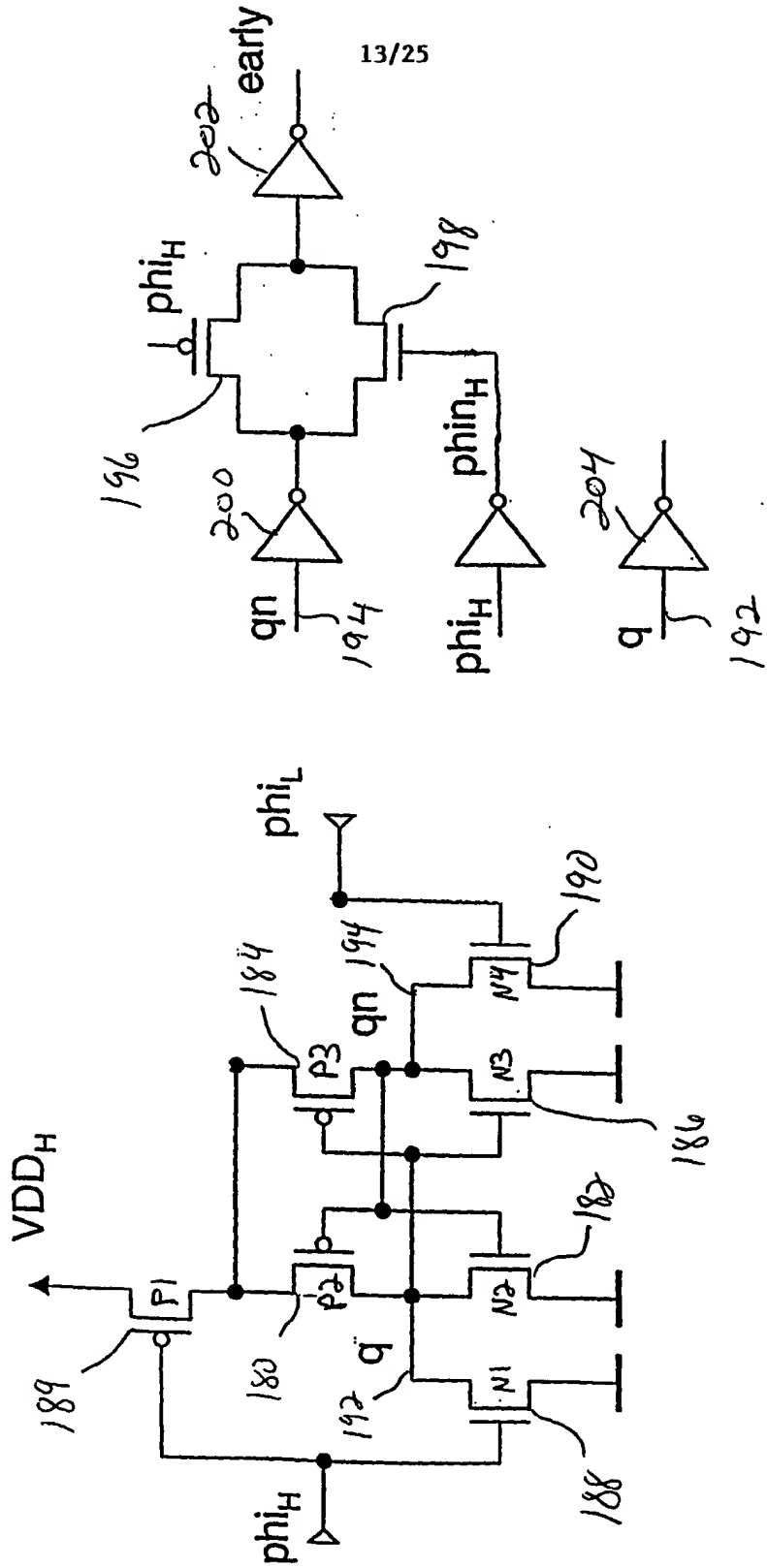


Fig. 10

14/25

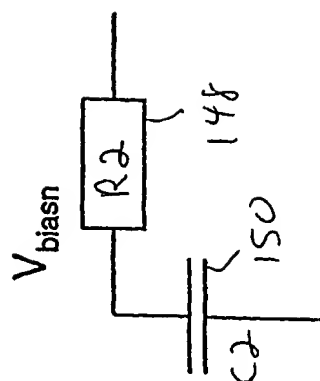
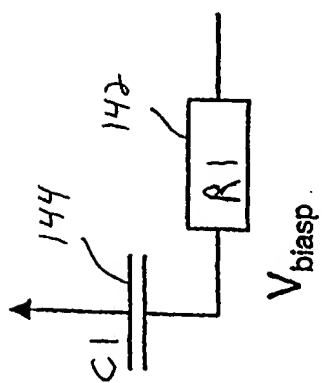
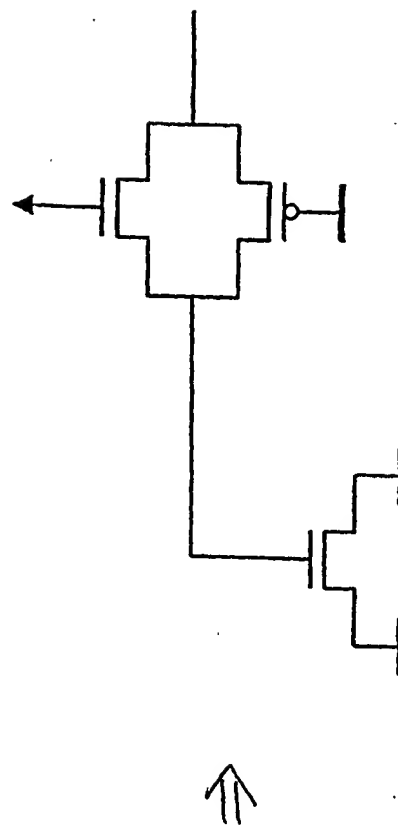
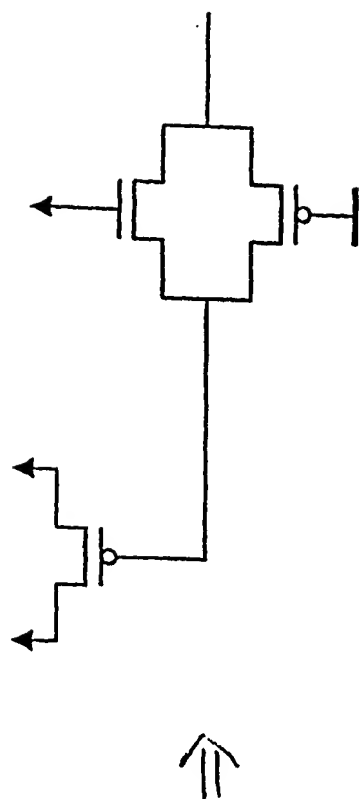


Fig. 11

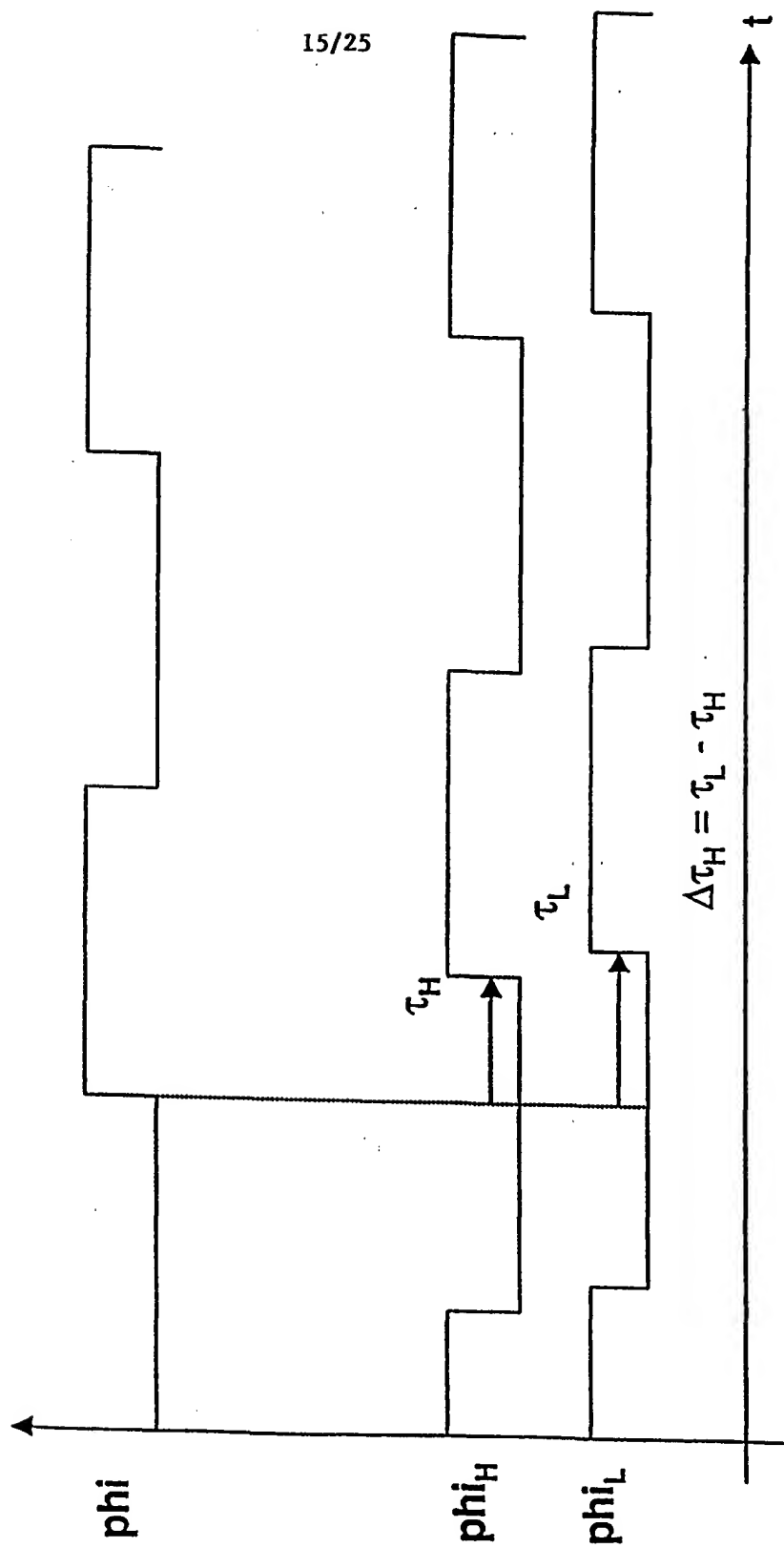
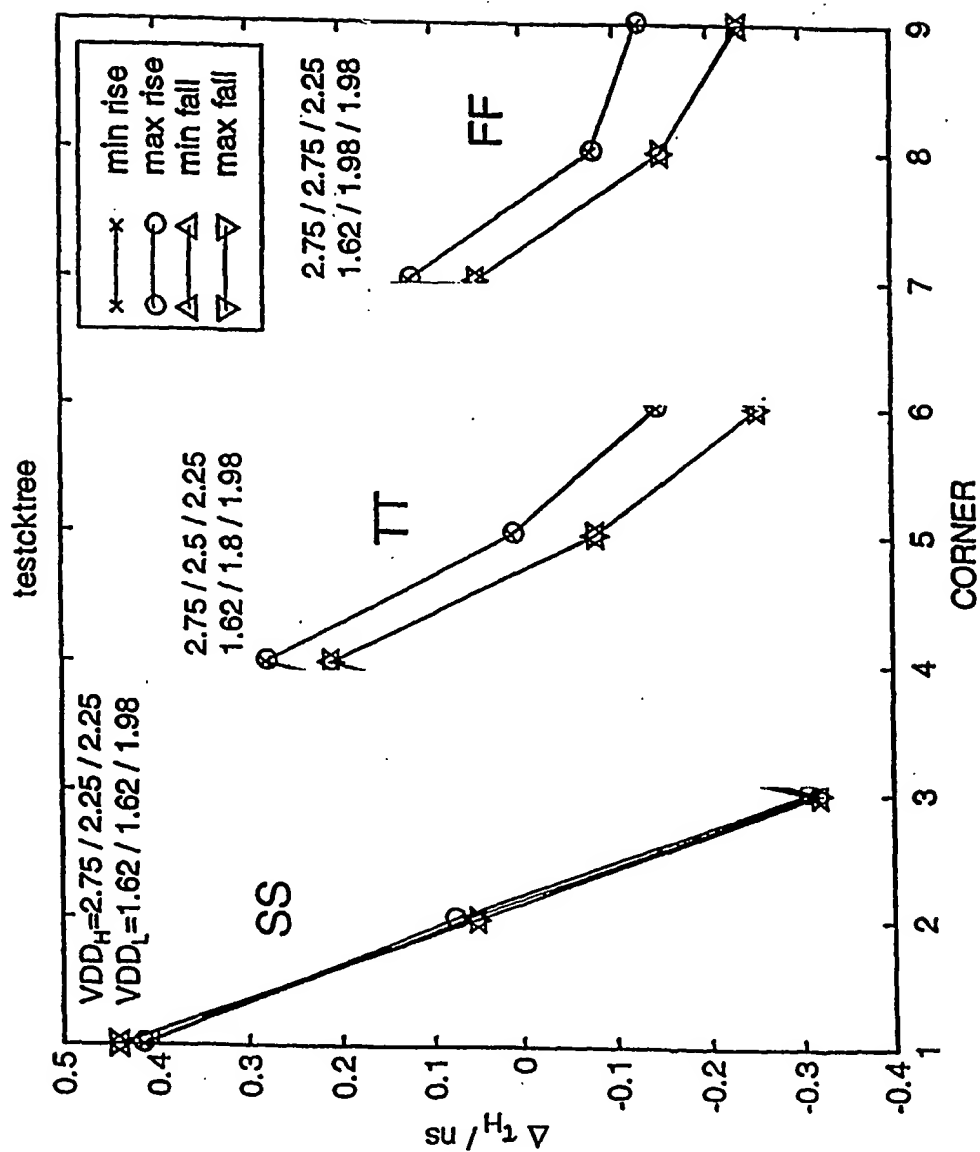


Fig. 12

16/25

Fig. 13A



17/25

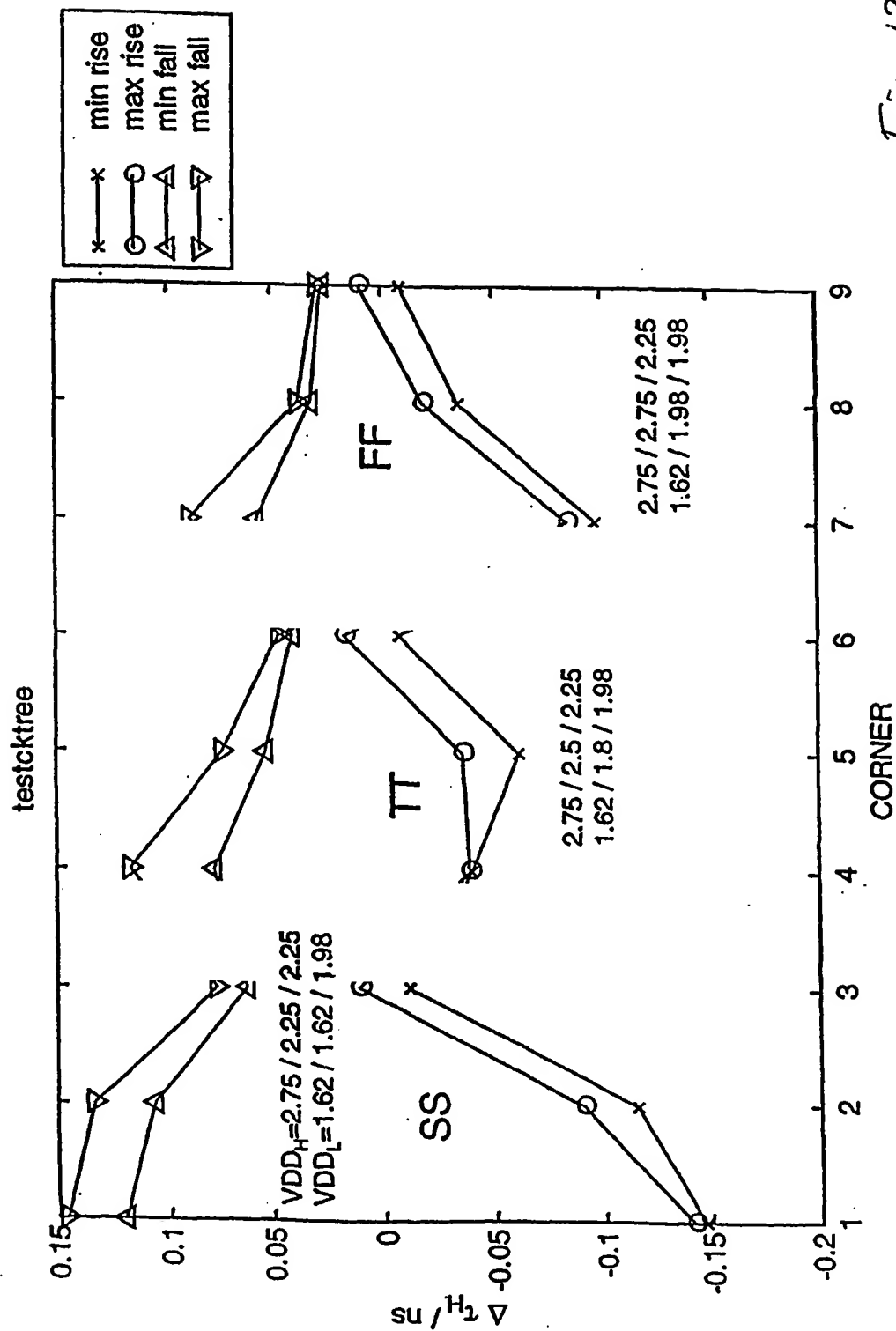


Fig. 13B

18/25

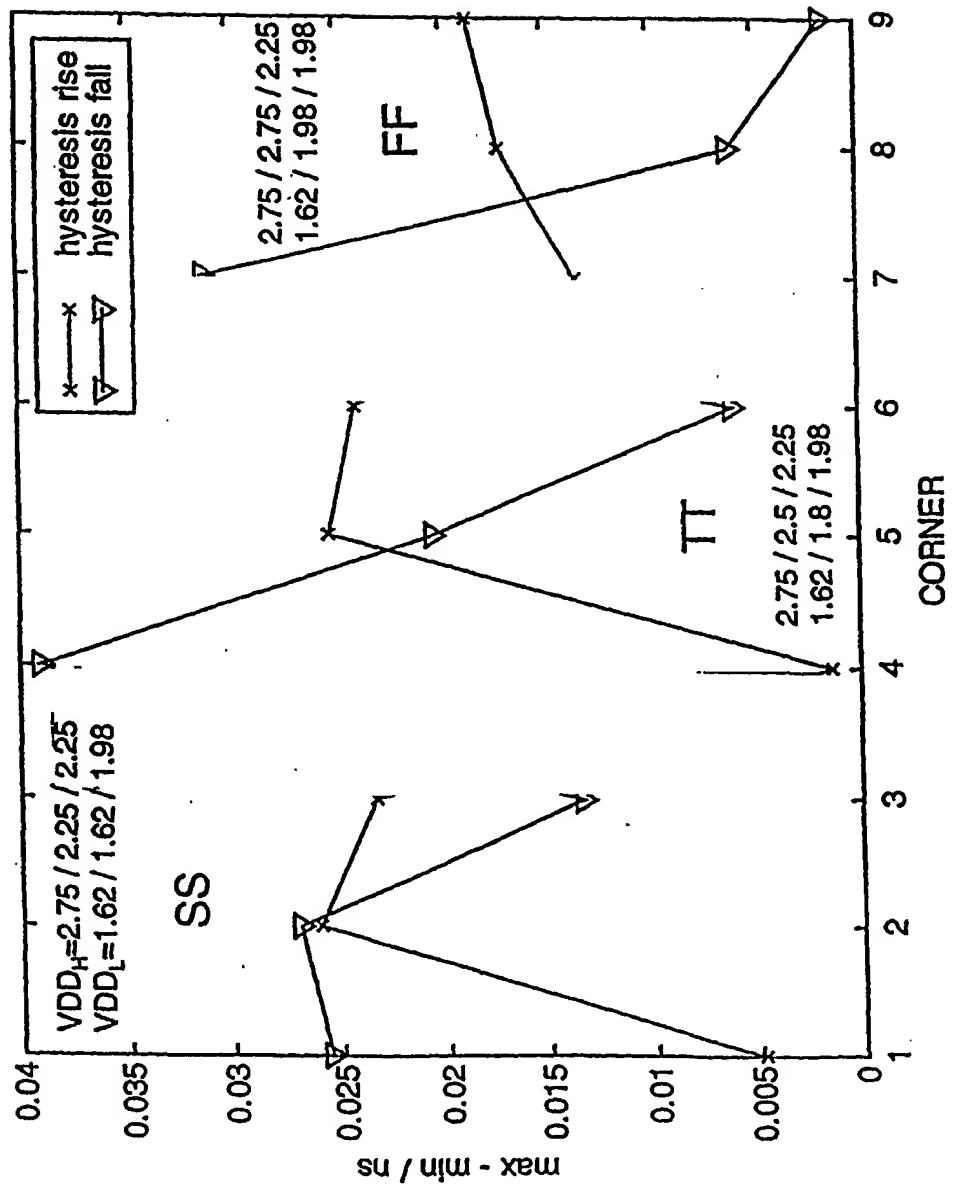


Fig. 13C

19/25

Fig. 13D

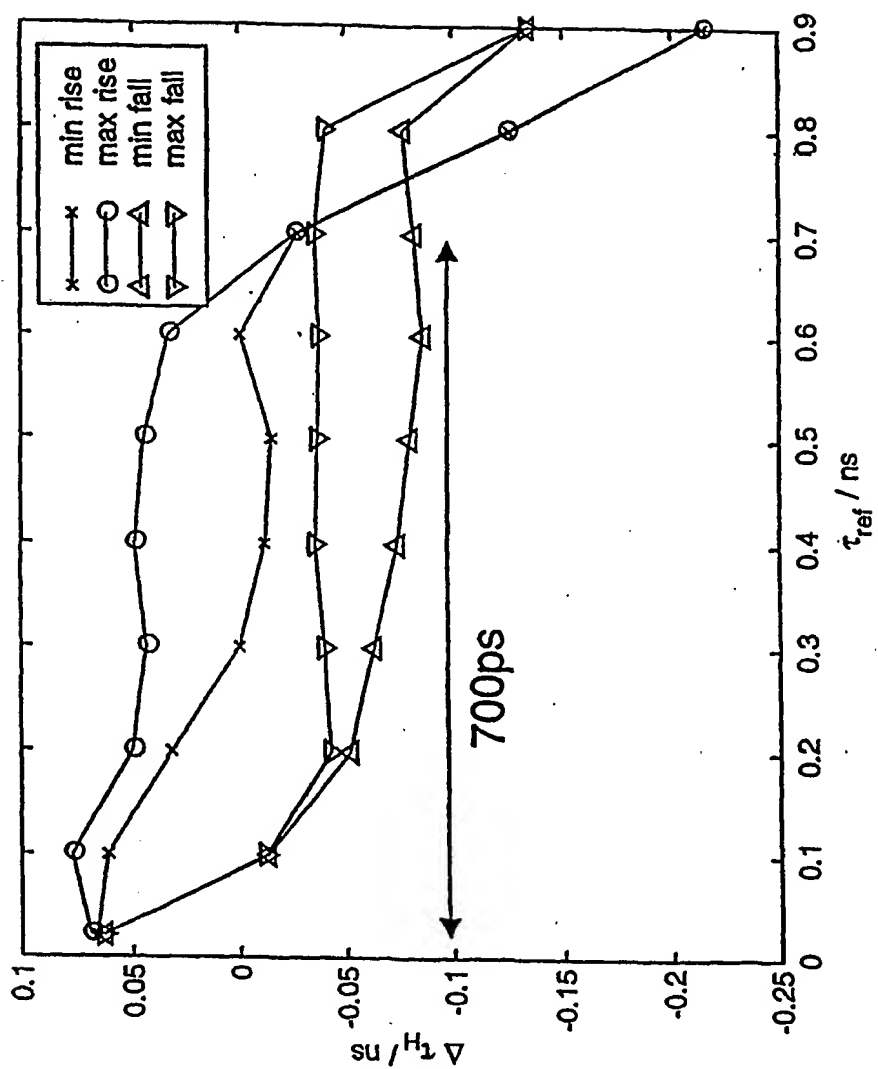
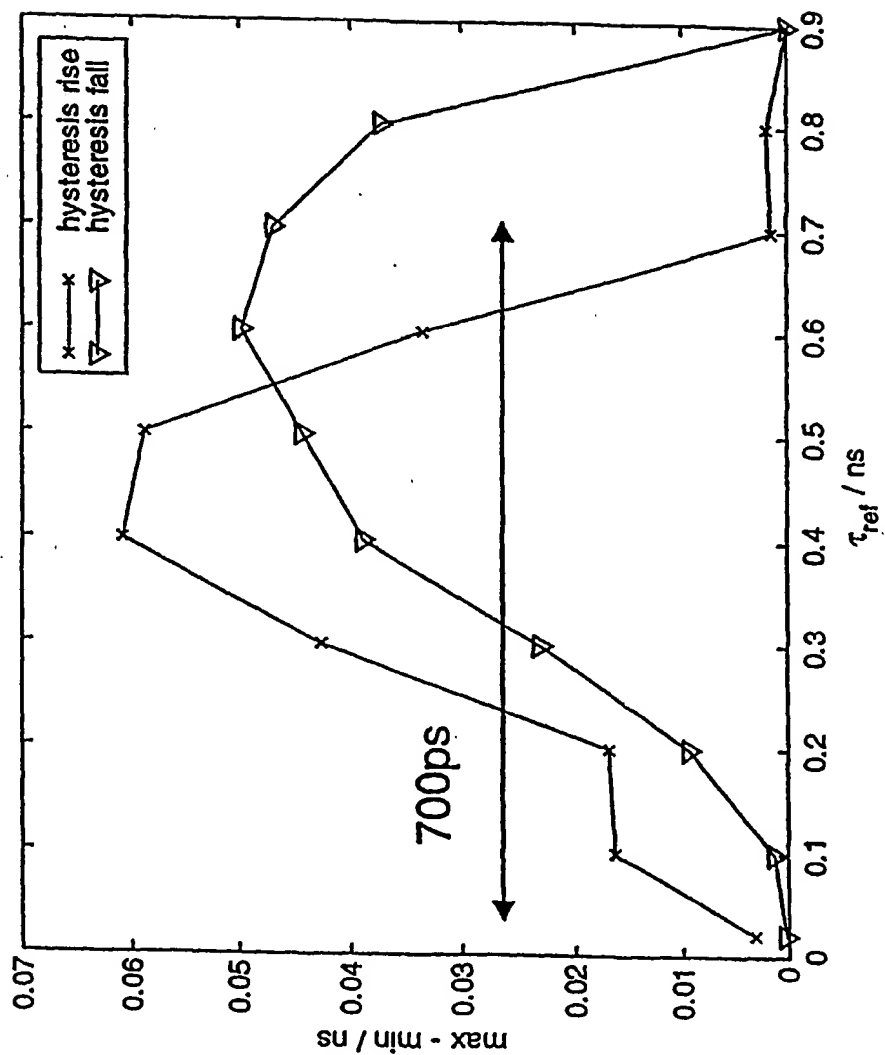


Fig. 13E



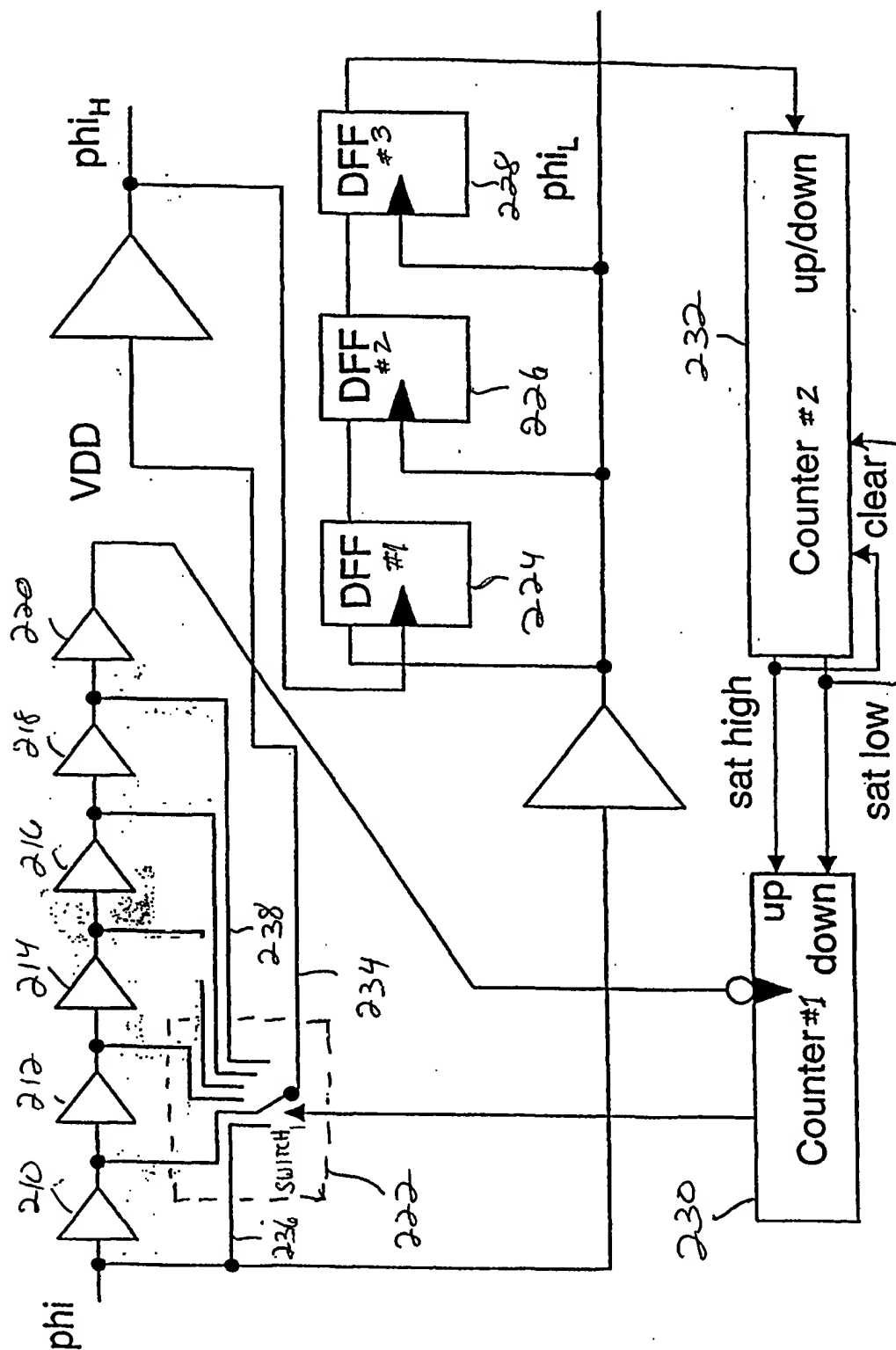


Fig. 14

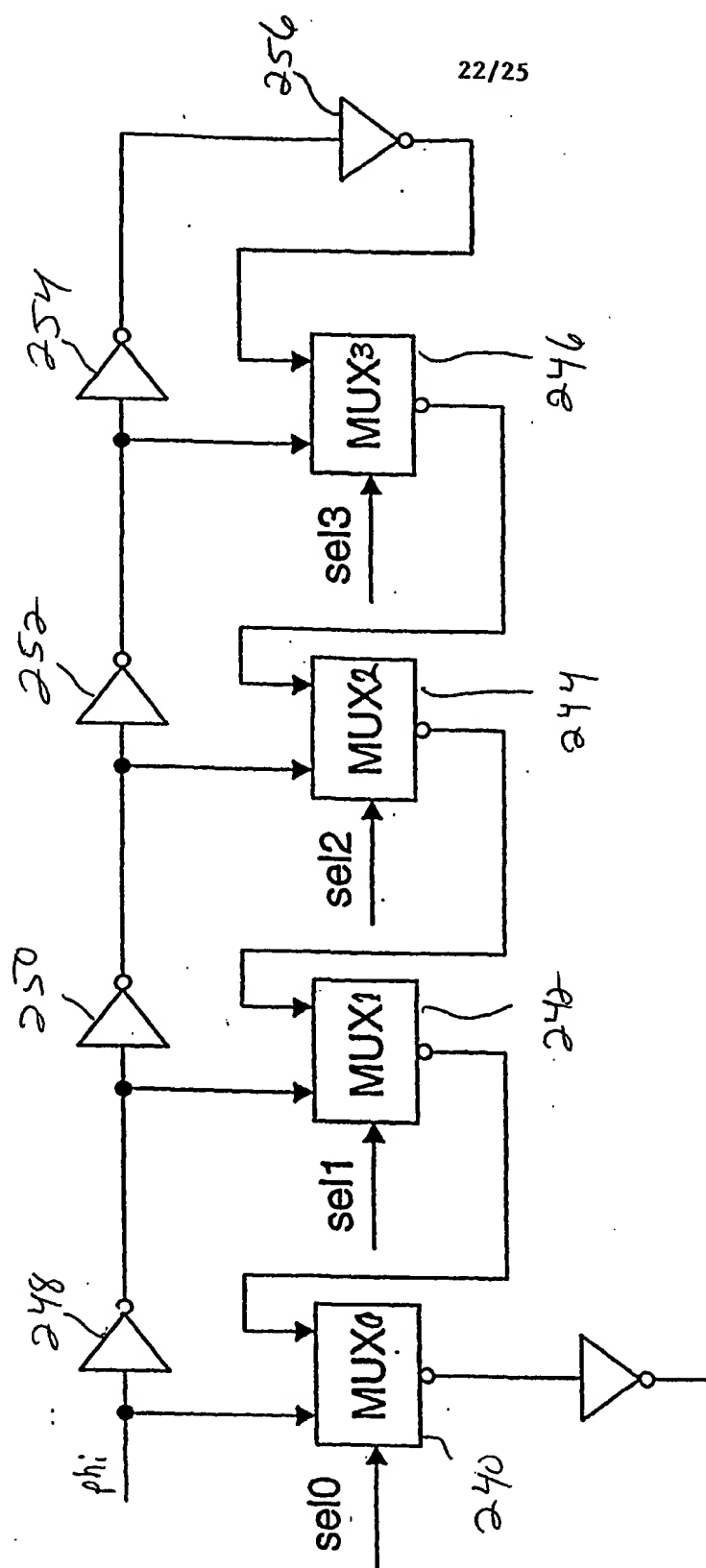


Fig. 15

23/25

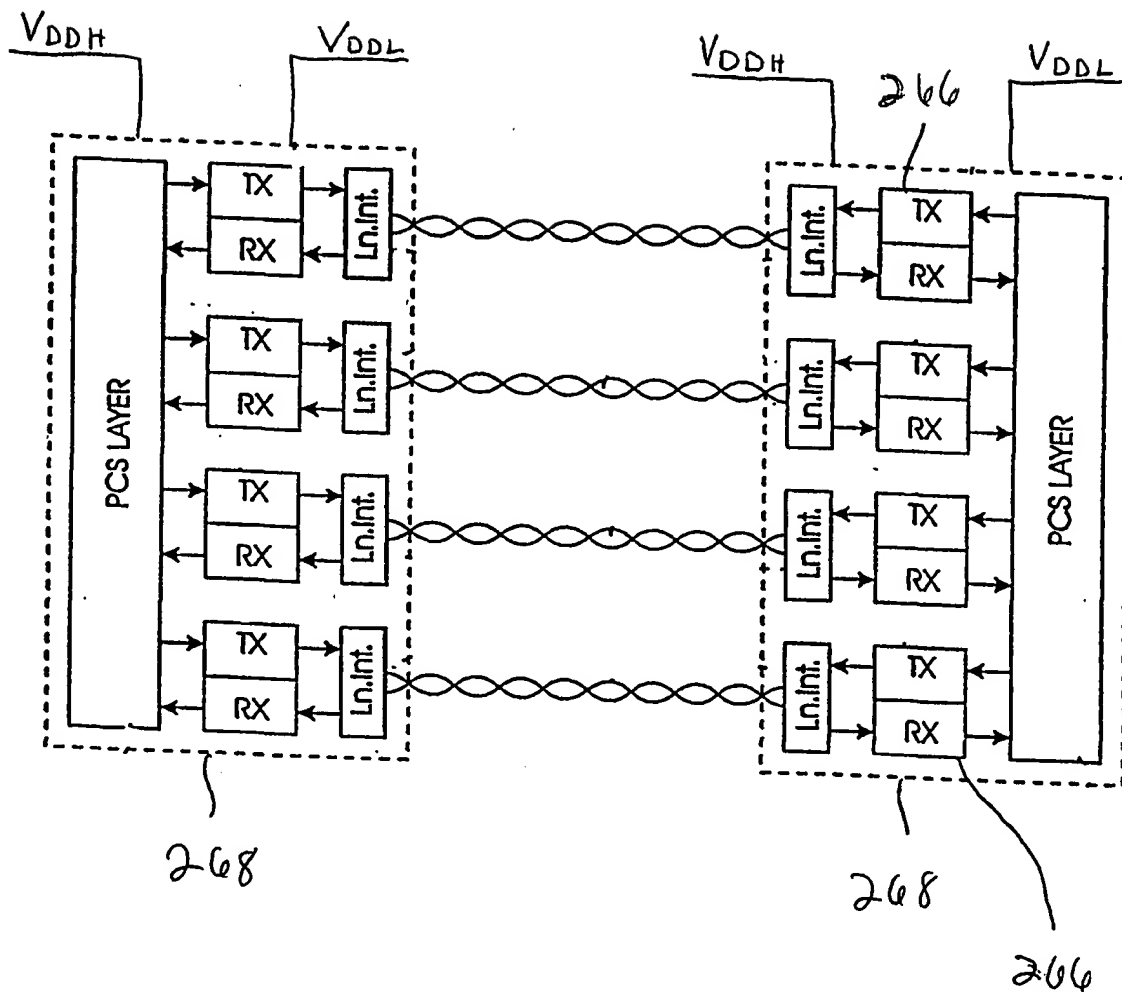


Fig. 16

24/25

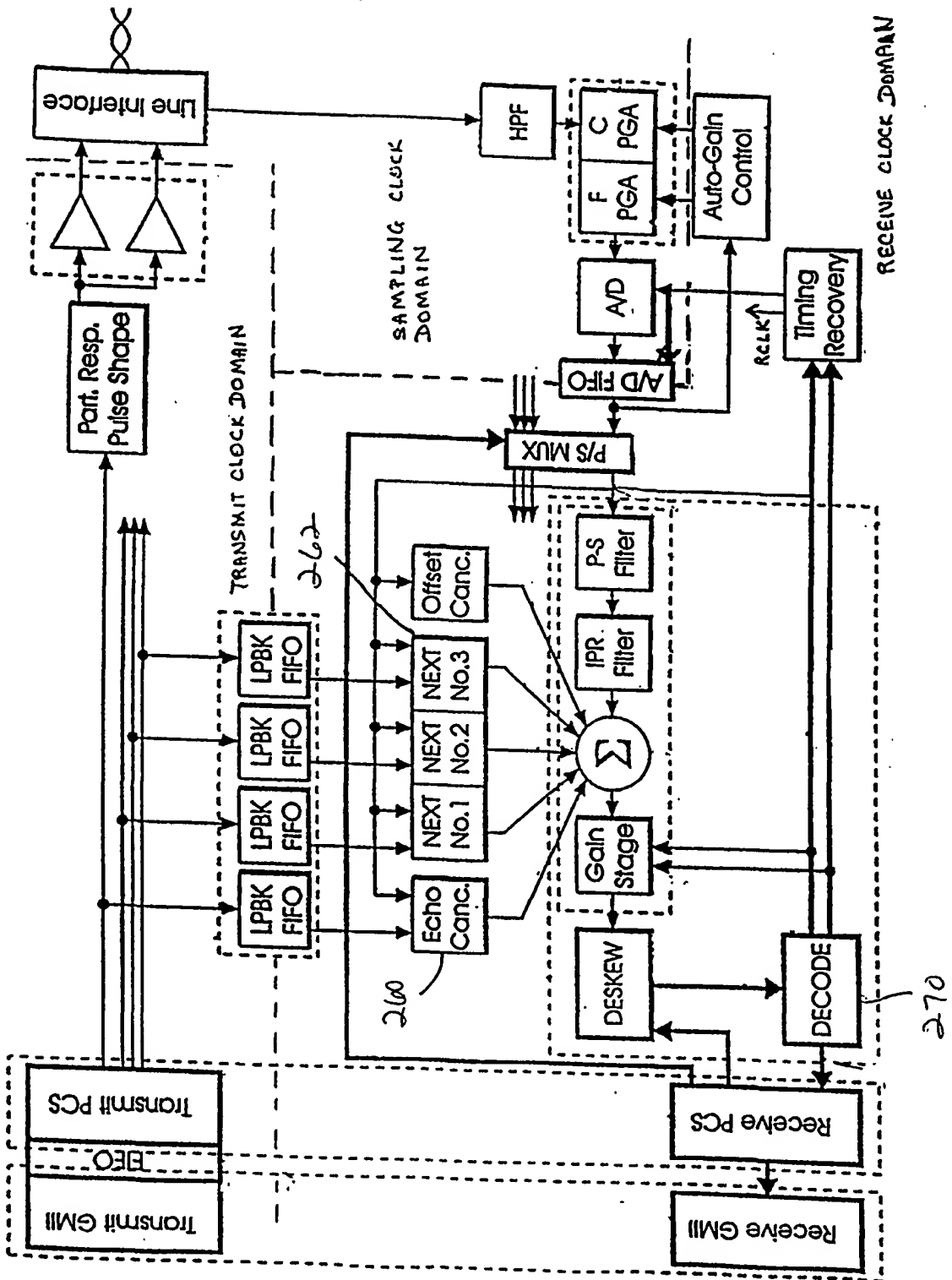


Fig. 17

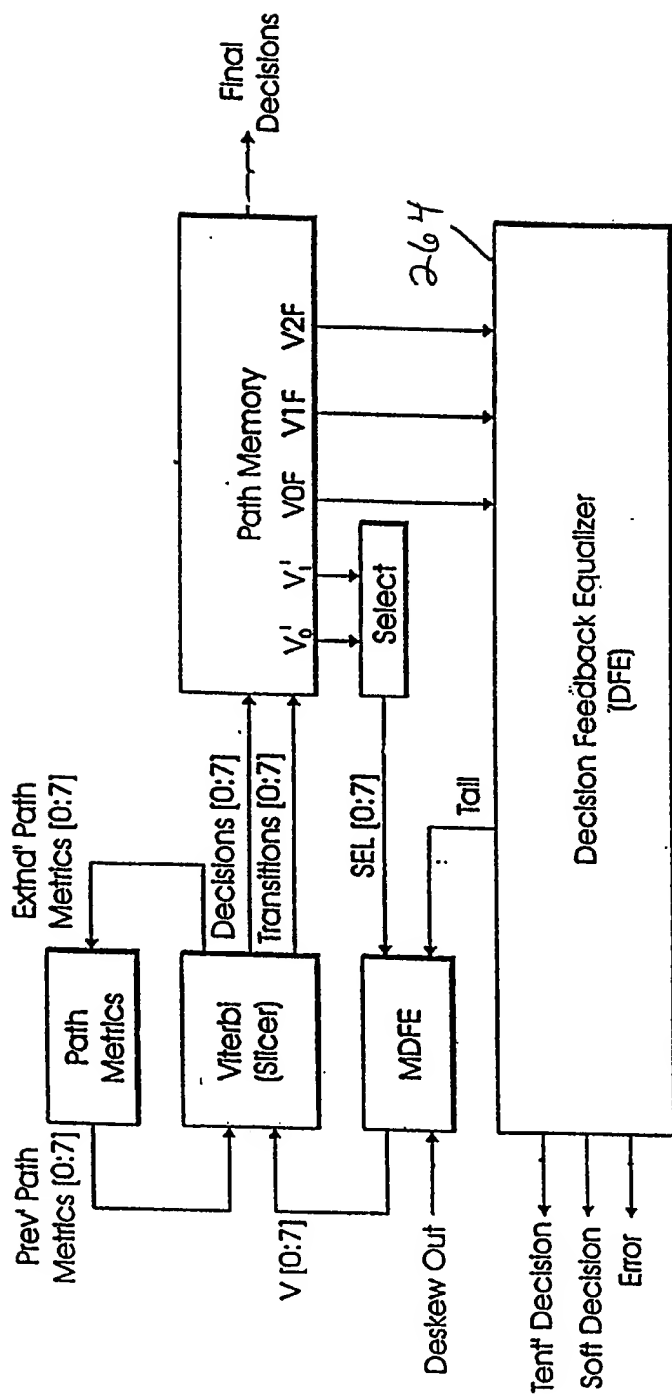


Fig. 18

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
26 July 2001 (26.07.2001)

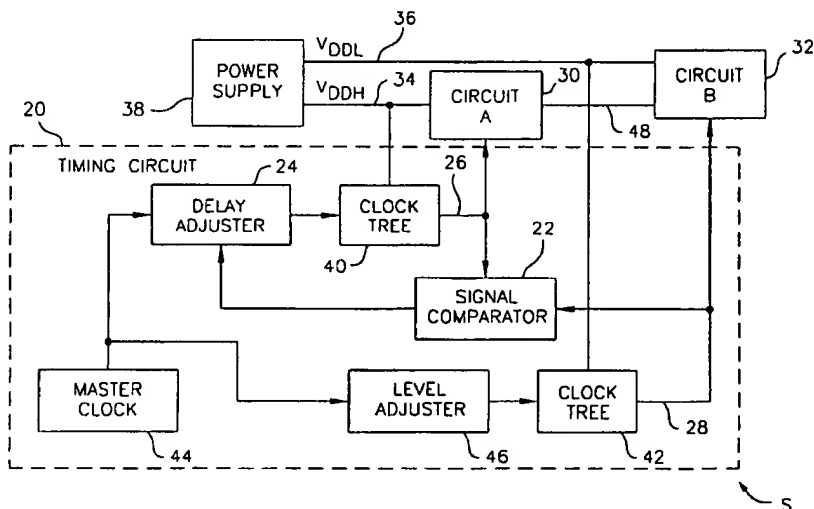
PCT

(10) International Publication Number
WO 01/53916 A3

- (51) International Patent Classification⁷: **G06F 1/10**, H03L 7/081
- (21) International Application Number: PCT/US01/02642
- (22) International Filing Date: 24 January 2001 (24.01.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/177.776 24 January 2000 (24.01.2000) US
60/182.421 14 February 2000 (14.02.2000) US
- (71) Applicant (for all designated States except US): **BROAD-COM CORPORATION** [US/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): **LUTKEMEYER, Christian, A., J.** [DE/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).
- (74) Agent: **WINSLADE, Christopher, C.**; McAndrews Held & Malloy, Ltd., Suite 3400, 500 W. Madison Street, Chicago, IL 60661 (US).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
- Declaration under Rule 4.17:**
— of inventorship (Rule 4.17(iv)) for US only
- Published:**
— with international search report

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR COMPENSATING FOR SUPPLY VOLTAGE INDUCED SIGNAL DELAY MISMATCHES



(57) Abstract: Various systems and methods providing signal delay compensation for circuits such as a multi-pair gigabit Ethernet transceiver are disclosed. In an analog implementation a buffer with an adjustable delay may be used to minimize the delay mismatch between clock trees. The delay of the adjustable-delay buffer is controlled by bias voltages that determine the charging and discharging current to the adjustable buffer. A phase detector circuit is used to compare the clock phases for rising and falling edges, and to adjust the bias voltages that control these edges. In a digital implementation a selector switch, responsive to a phase detector, may be used to route clock signals through circuit elements to delay clock signals.



(88) Date of publication of the international search report:
2 May 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(15) Information about Correction:

Previous Correction:

see PCT Gazette No. 40/2001 of 4 October 2001, Section II

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/02642

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F1/10 H03L7/081

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 900 752 A (MAR MONTE F) 4 May 1999 (1999-05-04) column 2, paragraph 3; figure 3 -----	1,2,10, 11,15, 22,26 18



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *8* document member of the same patent family

Date of the actual completion of the international search

16 October 2001

Date of mailing of the international search report

26/10/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Ciarelli, N

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internal Application No	
-------------------------	--

PCT/US 01/02642

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5900752	A	04-05-1999	NONE

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
26 July 2001 (26.07.2001)

PCT

(10) International Publication Number
WO 01/53916 A2

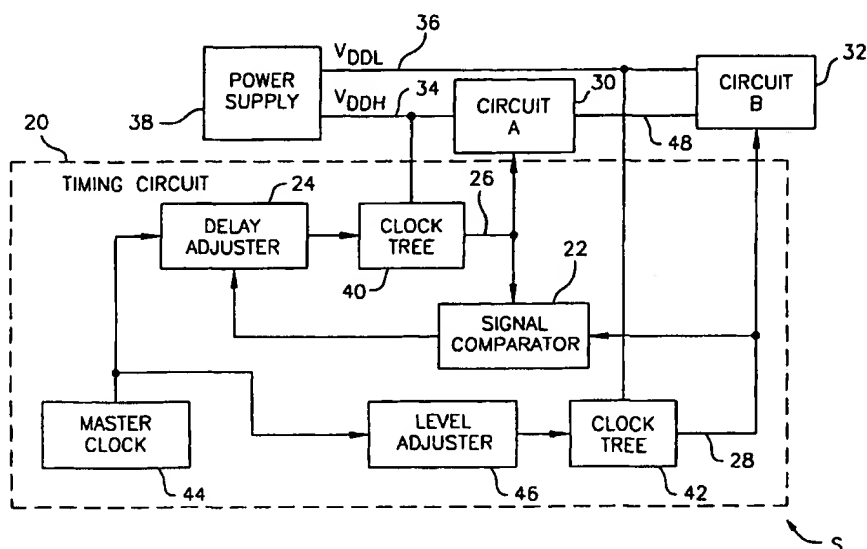
- (51) International Patent Classification⁷: G06F 1/10 (74) Agent: BURBACH, Stephen, D.; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).
- (21) International Application Number: PCT/US01/02642
- (22) International Filing Date: 24 January 2001 (24.01.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/177,776 24 January 2000 (24.01.2000) US
60/182,421 14 February 2000 (14.02.2000) US
- (71) Applicant (for all designated States except US): BROAD-COM CORPORATION [US/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): LUTKEMEYER, Christian, A., J. [DE/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— of inventorship (Rule 4.17(iv)) for US only

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR COMPENSATING FOR SUPPLY VOLTAGE INDUCED SIGNAL DELAY MISMATCHES



(57) Abstract: Various systems and methods providing signal delay compensation for circuits such as a multi-pair gigabit Ethernet transceiver are disclosed. In an analog implementation a buffer with an adjustable delay may be used to minimize the delay mismatch between clock trees. The delay of the adjustable-delay buffer is controlled by bias voltages that determine the charging and discharging current to the adjustable buffer. A phase detector circuit is used to compare the clock phases for rising and falling edges, and to adjust the bias voltages that control these edges. In a digital implementation a selector switch, responsive to a phase detector, may be used to route clock signals through circuit elements to delay clock signals.

WO 01/53916 A2



Published:

— *without international search report and to be republished
upon receipt of that report*

(15) Information about Correction:

see PCT Gazette No. 40/2001 of 4 October 2001, Section
II

(48) Date of publication of this corrected version:

4 October 2001

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*